

# ***Kylo-2 (LKL-2)***

## ***Whiskeylake-U Schematics***

**Project Code: 4PD0FC010001**  
**PCB(Raw Card): 18724-1M**

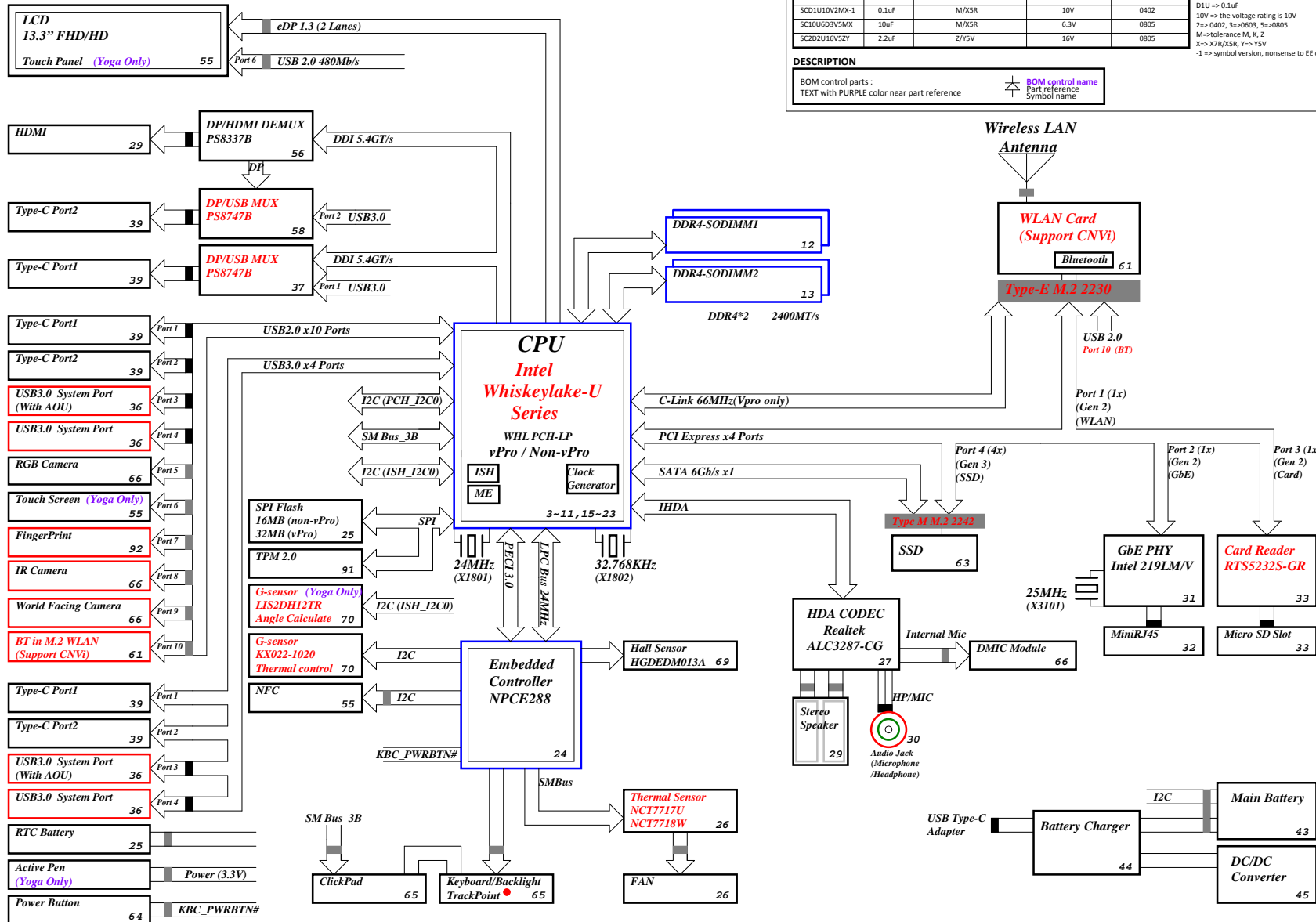
***2018-10-17***

LKL-2

<b>緯創資通</b>			<b>Wistron Corporation</b>		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>COVER PAGE</b>					
Size A4	Document Number <b>Kylo-2</b>				Rev <b>1M</b>
Date:	Wednesday, October 17, 2018		Sheet	1	of 99

# Kylo-2 Whiskeylake Block Diagram

Project Code: 4PD0FC010001  
PCB(Raw Card): 18724-1M



- External Connector/Socket
- Internal Connector/Socket
- Internal Switch

RESISTOR					
Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1%)	Rating	Size	
0402	1/16W, 25V		0402 => 1/16W, 25V	2-->0402, 3-->0603, 5-->0805, 6-->1206, 0-->1210	
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603	
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805	
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603	

CAPACITOR					
Symbol name	Value	Tolerance (M: +/-20%, K: +/-10%, Z: +80/-20%)	Rating	Size	
SCD1U10V2M0K-1	0.1uF	M/XSR	10V	0402	
SC10U6D3V5M0K	10uF	M/XSR	6.3V	0805	
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805	

**DESCRIPTION**  
BOM control parts :  
TEXT with PURPLE color near part reference

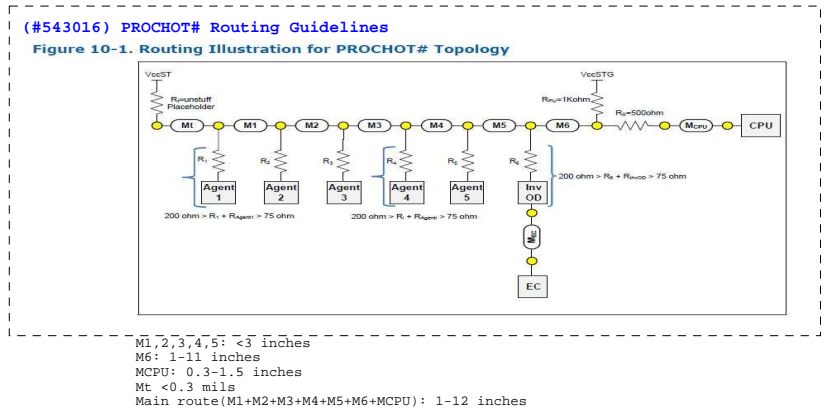
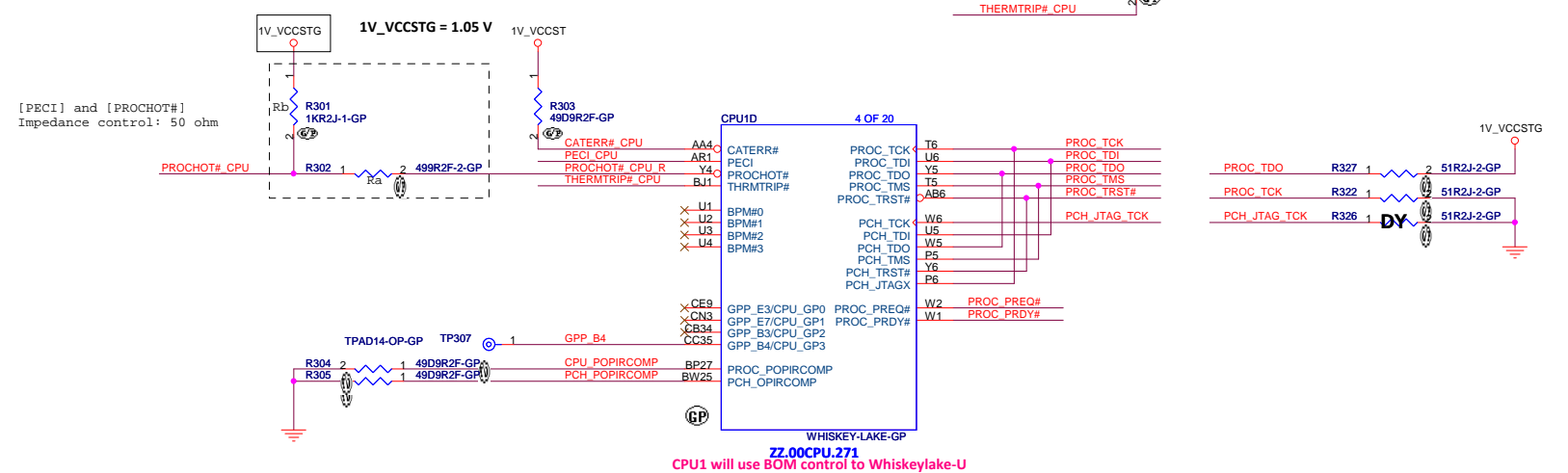
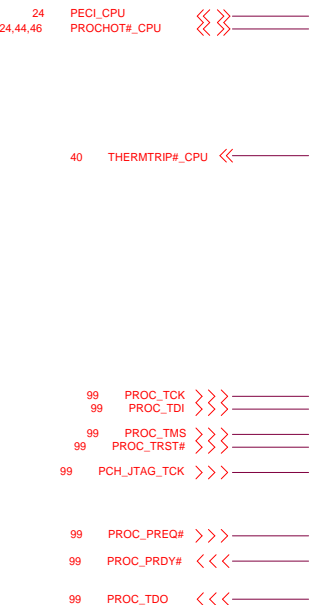
The naming rule is value + R + size + tolerance  
For the value, it can be read by the number before R. (R means resistor)  
For the tolerance, it can be read from the last letter.  
For the rating, we don't show on the symbol name.  
For the size, R2-->0402, R3-->0603, R5-->0805,....

The naming rule is  
Capacitor type + value + rating + size + tolerance + material  
SCD1U10V2M0K-1  
SC-->SMT Ceramic, TC--> POS cap or SP cap  
DIU --> 0.1uF  
10V --> the voltage rating is 10V  
2--> 0402, 3-->0603, 5-->0805  
M-->tolerance M, K, Z  
X-->X7R/X5R, Y-->Y5V  
-1 --> symbol version, nonsense to EE characteristic

PCB Layer Stackup	
8 Layers FR4	
L1:Component	
L2:GND	
L3:Signal 1	
L4:VCC	
L5:Signal 2	
L6:Signal 3	
L7:VCC	
L8:Component	

Battery Charger/Selector	
VINT20_IN	44
19V_DCBATOUT	BT+
System DC/DC	
TP5S1225BRUKR	45
19V_DCBATOUT	5V_SS
3D3V_SS	
IMVP8 Controller	
NCP81218MNTXG	46
19V_DCBATOUT	5V_CPU_CORE
DC/DC VCCCPUCORE	
NCP302045MNTXG	47
19V_DCBATOUT	1V_CPU_CORE
DC/DC VCCGT	
NCP302035MNTXG	48
19V_DCBATOUT	1V_VCCGT
DC/DC VCCSA	
NCP81253MNTBG	50
19V_DCBATOUT	1V_VCCSA
DC/DC DDR4 VDDQ	
RT8231AGQW	51
19V_DCBATOUT	ID2V_S3
DC/DC DDR4 VTT	
RT8231AGQW	51
ID2V_S3	6D6V_YREF_S0
DC/DC DDR4 VPP	
RT5797ALGQW	51
3D3V_SS	2D5V_SS
DC/DC ID05V_S5	
RT8231AGQW	52
19V_DCBATOUT	ID0V_S5
DC/DC ID8V_SUS	
RT5797ALGQW	53
3D3V_SS	ID8V_SUS

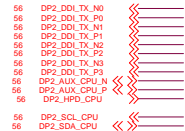
Main Func = CPU



USBC



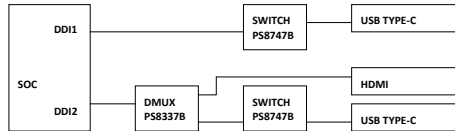
USBC



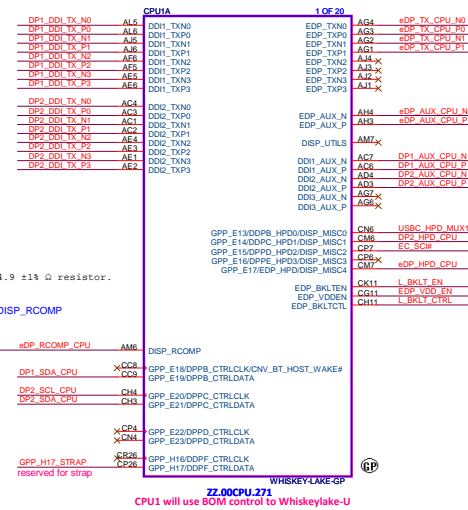
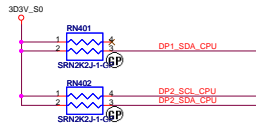
Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

TABLE: Functional Strap

DDPB_CTRLDATA
HIGH Port B is detected.
LOW Port B is not detected.
DDPC_CTRLDATA
HIGH Port C is detected.
LOW Port C is not detected.

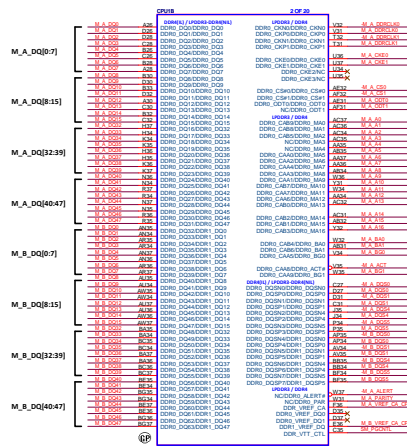
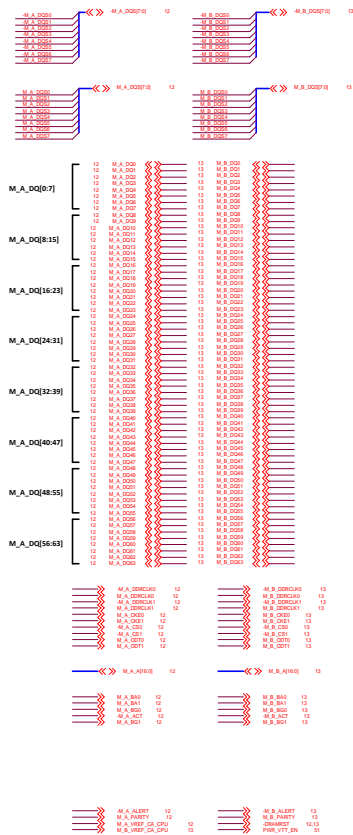


Design Guideline:  
Skylake processor signal eDP\_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

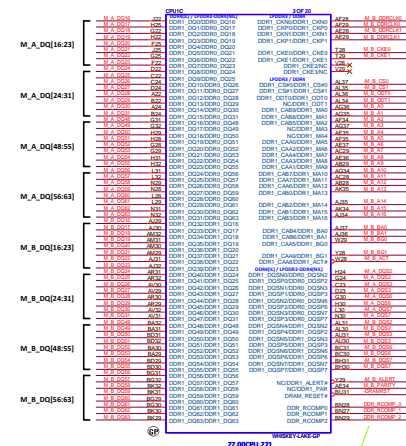
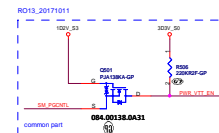


LKL-2

## DDR4 ball type: Non-Interleaved Type



CPU1 will use B0M control to Whiskeylake-U  
 Check DQ and CQ and DQ and DQ differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.



CPU1 will use B0M control to Whiskeylake-U

Layout Note:  
 Table 4.3. WHL U DDR4 SDRAM Signal Routing Guidelines (mils)  
 Design Guideline:  
 SR, RCOMP, S1/2 keep routing length less than 500 mils.

Table 3-1. RCOMP Recommendation for WHL and CPL  
 DDR - DDR4 SDRAM  
 DDR, RCOMP[0]: 121Ω ±1% on plug to VSS  
 DDR, RCOMP[1]: 80.6Ω ±1% on plug to VSS  
 DDR, RCOMP[2]: 100Ω ±1% on plug to VSS

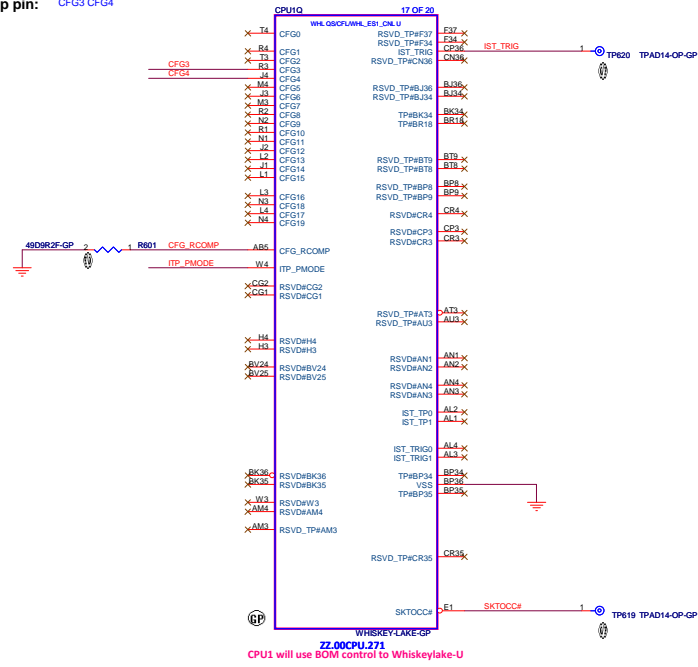


RL2-2

15,99 CFG3 <<< CFG3  
15 CFG4 <<< CFG4

99 ITP\_PMODE <<<

PCH strap pin: CFG3 CFG4

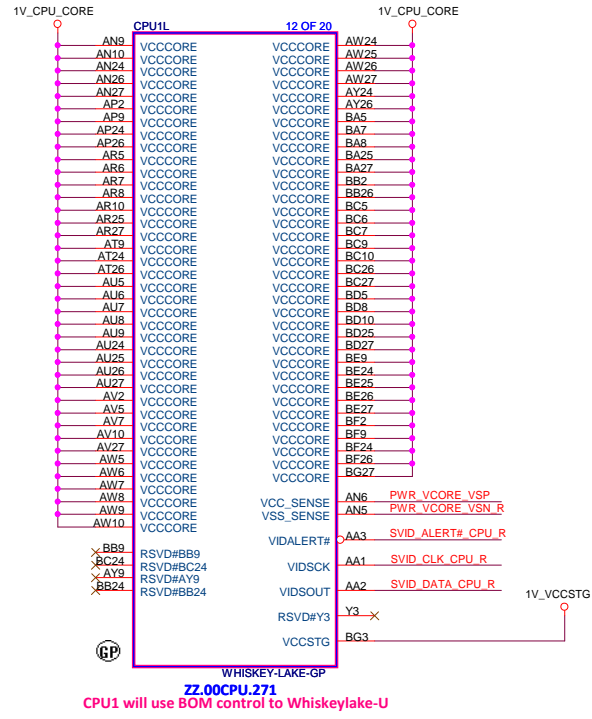


ZZ.00CPU.271  
CPU1 will use BOM control to Whiskeylake-U

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Main Func = CPU

46 PWR\_VCORE\_VSP <<=====  
46 PWR\_VCORE\_VSN\_R <<=====  
46 PWR\_VCORE\_ALERT# <<=====  
46 VIDSCK\_CPU\_R <<=====  
46 VIDSOUT\_CPU\_R <<=====



ZZ.00CPU.271  
CPU1 will use BOM control to Whiskeylake-U

Figure 10-7. Routing Illustration for SVID Topology

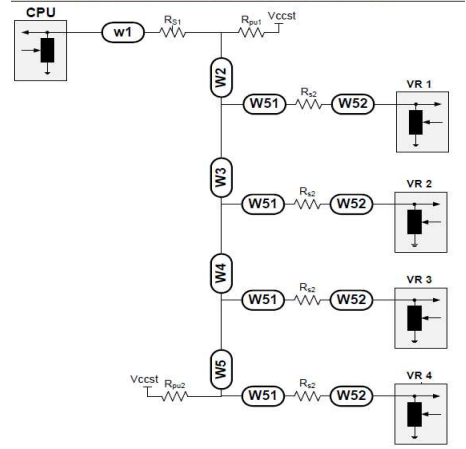
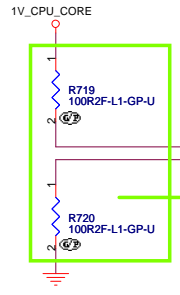


Table 10-10. SVID Bus Routing Guidelines

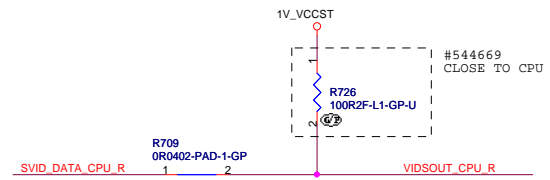
Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R <sub>DS1</sub> [Ω]	R <sub>DS2</sub> [Ω]	R <sub>S1</sub> [Ω]	R <sub>S2</sub> [Ω]	VCC <sub>PT</sub> [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	



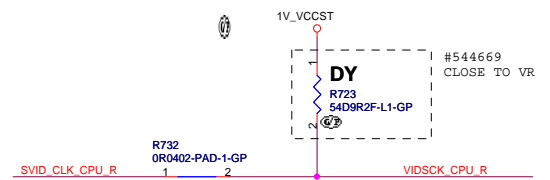
- Layout Note:
1. Place close to CPU
  2. VCC\_SENSE/ VSS\_SENSE impedance=50 ohm
  3. Length match<25mil

Layout Note:  
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).  
Route the Alert signal between the Clock and the Data signals.

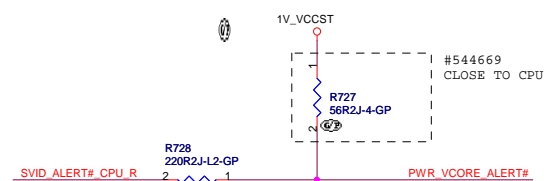
SVID DATA



SVID CLOCK



SVID ALERT



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Title CPU (VCC\_CORE)

Size A3 Document Number Kylo-2 Rev 1M

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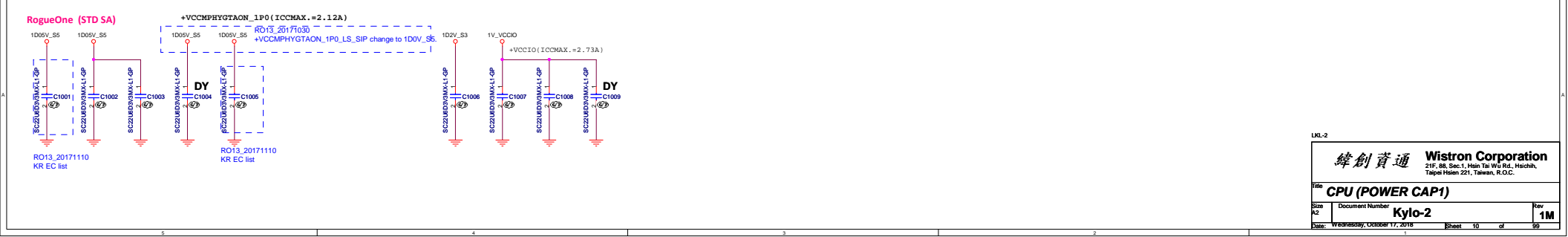


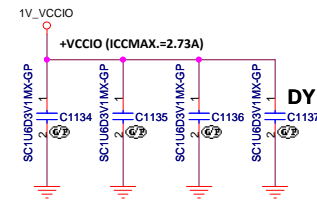


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Title <b>CPU (RSVD)</b>		
Size A4	Document Number <b>Kylo-2</b>	Rev <b>1M</b>
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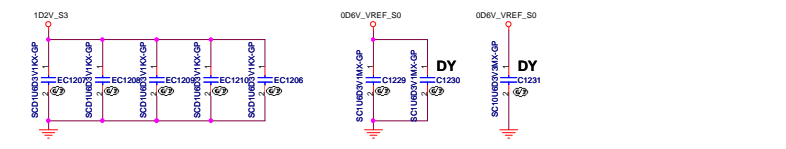
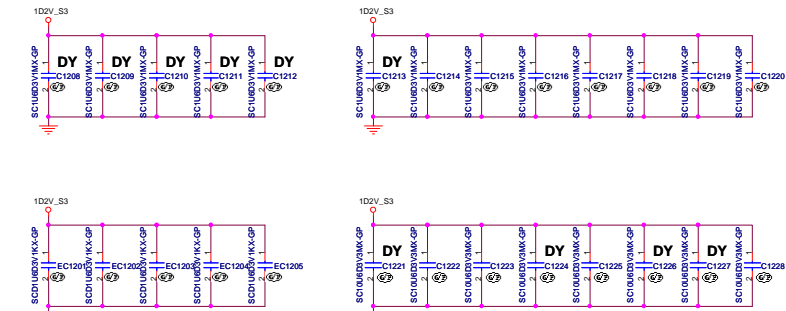
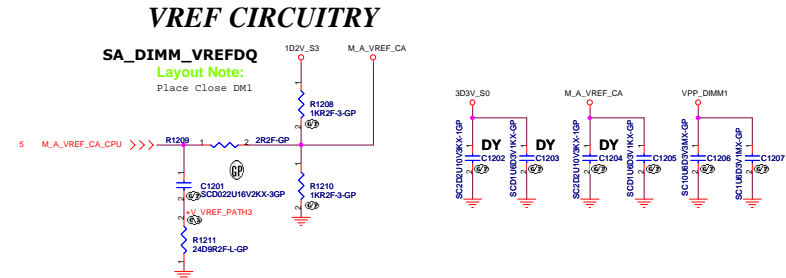


KL2\_SIT\_MB\_W006

**SPD Address of DM1**

SPD SA2	0
SPD SA1	0
SPD SA0	0

Note:  
SA0 DM1 = 0, SA1\_DM1 = 0  
SA2 DM1 = 0  
SO-DIMMA SPD Address is 0xA0



KL2\_SIT\_MB\_W006

### SPD Address of DM2

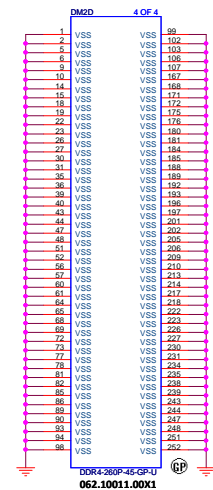
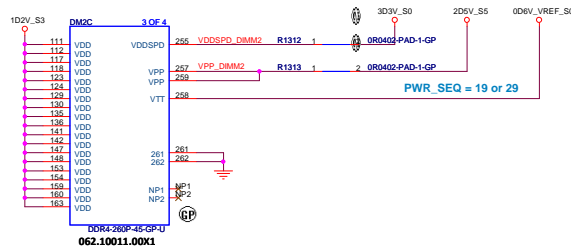
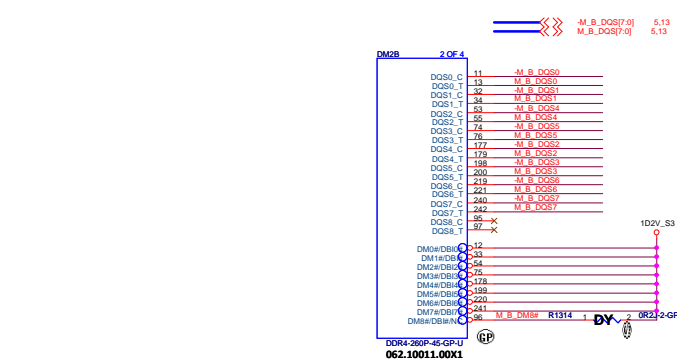
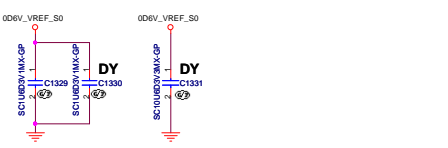
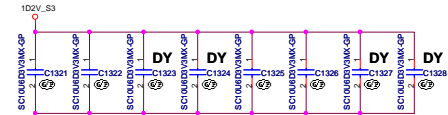
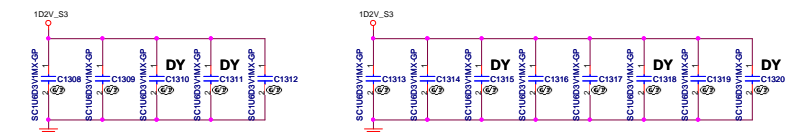
Diagram (a) shows the SPD address configuration for SA0. The diode is connected to SA0, and the pull-up resistor is R1302. The DIMM SPD pin is labeled DM2-SA0=0.

Diagram (b) shows the SPD address configuration for SA1. The diode is connected to SA1, and the pull-up resistor is R1303. The DIMM SPD pin is labeled DM2-SA1=0.

Diagram (c) shows the SPD address configuration for SA2. The diode is connected to SA2, and the pull-up resistor is R1304. The DIMM SPD pin is labeled DM2-SA2=1.

SPD SA2	0
SPD SA1	0
SPD SA0	1





















Note:  
 SA0 DM2 = 1, SA1\_DM2 = 0  
 SA2 DM2 = 0  
 SO-DIMM SPD Address is 0xA2

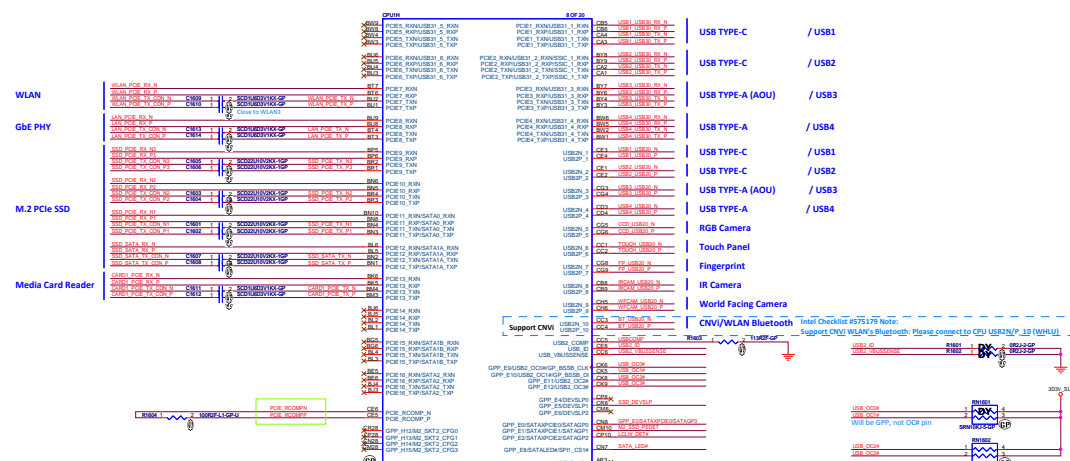
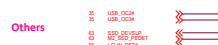
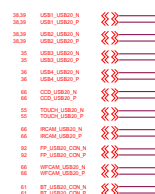
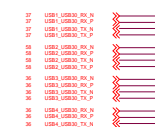
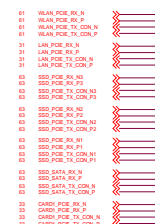
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LKL-2

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Title DDR (RSVD)		
Size A4	Document Number Kylo-2	Rev 1M
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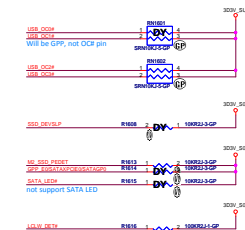
<b>HW Strap</b> 				<b>GPP_B14 / SPWR</b> Top Strap Override Rising edge of PCH_PWROK <p>This signal has a weak internal pull-down. 0 = <b>Enable</b> "Top Strap" mode. (Default) 1 = <b>Disable</b> "Top Strap" mode. This mode is an address decoder feature that enables the external device to be used as a strap override. This mode is only supported when the external device is connected to the PCH_PWROK pin.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after the strap sampling.</li><li>Software will not be able to clear the Top Strap bit until the strap is configured to 0.</li><li>The strap bit will be cleared after the strap sampling.</li><li>This signal is in the primary well.</li></ol>				<b>GPP_B18 / GSP10_MOSI</b> No Reboot Rising edge of PCH_PWROK <p>This signal has a weak internal pull-down. 0 = <b>Disable</b> "No Reboot" mode. (Default) 1 = <b>Enable</b> "No Reboot" mode (PCH will disable the TCO timer system reboot feature). This function is useful when running ITP/XDP.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after PCH_PWROK is high.</li><li>This signal is in the primary well.</li></ol>				<b>GPP_C2 / SMBALERT#</b> TLS Confidentiality Rising edge of RSMRST# <p>This signal has a weak internal pull-down. 0 = <b>Disable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = <b>Enable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after RSMRST# de-asserts.</li><li>This signal is in the primary well.</li></ol>				<b>GPP_B22</b> Rising edge of RSMRST# <p>This signal has a weak internal pull-down. 0 = <b>Disable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = <b>Enable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after RSMRST# de-asserts.</li><li>This signal is in the primary well.</li></ol>			
<b>GPP_B14</b> 				<b>GPP_B18</b> 				<b>GPP_C2</b> 				<b>GPP_B22</b> 							
<b>GPP_C5 / SMLALERT#</b> eSPI or LPC Rising edge of RSMRST# <p>This signal has a weak internal pull-down. 0 = <b>LPC</b> is selected (for EC). (Default) 1 = <b>eSPI</b> is selected (for EC).</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after RSMRST# de-asserts.</li><li>This signal is in the primary well.</li></ol> <p><b>Warning:</b> If this strap is configured to 0 (eSPI is disabled), the eSPI Flash Sharing Mode strap must be configured to 1 as well (SAFS is disabled).</p>				<b>SP10_MOSI</b> Reserved Rising edge of RSMRST# <p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>				<b>GPP_D12 / ISH_SPI_MOSI / GSP12_MOSI</b> Reserved Rising edge of RSMRST# <p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>				<b>GPP_B23 / SMLALERT# / PCHHOT#</b> Intel® DCI-OOB Rising edge of RSMRST# <p>This signal has an internal pull-down. 0 = <b>Disable</b> Intel® DCI-OOB (Default) 1 = <b>Enable</b> Intel® DCI-OOB</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after RSMRST# de-asserts.</li><li>When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.</li><li>This signal is in the primary well.</li></ol>							
<b>GPP_C5</b> 				<b>SP10_MOSI</b> 				<b>GPP_D12</b> 				<b>GPP_B23</b> 							
<b>SP10_I02</b> Reserved Rising edge of RSMRST# <p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>				<b>SP10_I03</b> Reserved Rising edge of RSMRST# <p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>				<b>HDA_SDO / I2SD0_TXD</b> Flash Descriptor Security Override Rising edge of PCH_PWROK <p>This signal has a weak internal pull-down. 0 = <b>Enable</b> security measures defined in the Flash Descriptor. (Default) 1 = <b>Disable</b> Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after PCH_PWROK is high.</li><li>This signal is in the primary well.</li></ol>				<b>GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT</b> Display Port B Detected Rising edge of PCH_PWROK <p>This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal Pull-down is disabled after PCH_PWROK is high.</li><li>This signal is in the primary well.</li></ol>							
<b>SP10_I02</b> 				<b>SP10_I03</b> 				<b>GPP_R2 / HDA_SDO / I2SD0_TXD / HDACPU_SDO</b> 				<b>GPP_E19</b> 							
<b>GPP_E21 / DDPB_CTRLDATA</b> Display Port C Detected Rising edge of PCH_PWROK <p>This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal Pull-down is disabled after PCH_PWROK is high.</li><li>This signal is in the primary well.</li></ol>				<b>GPP_E23 / DDPB_CTRLDATA</b> Display Port D Detected Rising edge of PCH_PWROK <p>This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after PCH_PWROK is high.</li><li>This signal is in the primary well.</li></ol>				<b>GPP_H17</b> Reserved Rising edge of PCH_PWROK <p>This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after PCH_PWROK is high.</li><li>This signal is in the primary well.</li></ol>				<b>GPP_H21</b> XTAL Frequency Select Rising edge of RSMRST# <p>This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 MHz XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after RSMRST# de-asserts.</li><li>This signal is in the primary well.</li></ol>							
<b>GPP_E21</b> 				<b>GPP_E23</b> 				<b>GPP_H17</b> 				<b>GPP_H21</b> 							
<b>GPP_F6 / CNV_RGL_DT</b> M.2 CNV Mode Select Rising edge of RSMRST# <p>An external pull-up or pull-down is required. 0 = Integrated CNV enable. 1 = Integrated CNV disable.</p>				<b>INPUT3VSEL</b> 3.0V Select Input pin must always be driven to a valid logic level <p>External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% <b>Note:</b> This strap should only be used for specific targeted 1S battery systems.</p>				<b>GPD7</b> Reserved Rising edge of DSW_PWROK <p>External pull-up is required. Recommend 100K.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>				<b>GPP_H23</b> eSPI Flash Sharing Mode Rising edge of RSMRST# <p>This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after RSMRST# de-asserts.</li><li>This signal is in the primary well.</li></ol> <p><b>Warning:</b> This strap must be configured to 0 (SAFS is disabled) if the eSPI or LPC strap is configured to 0 (eSPI is disabled).</p>							
<b>GPP_F2 / CNV_RGL_DT / UART0_TXD</b> 				<b>INPUT3VSEL</b> 				<b>GPD7</b> 				<b>GPP_H23</b> 							
<b>GPP_F2 / CNV_RGL_DT / UART0_TXD</b> 				<b>INPUT3VSEL</b> 				<b>GPD7</b> 				<b>GPP_H23</b> 							



**Layout Note:**

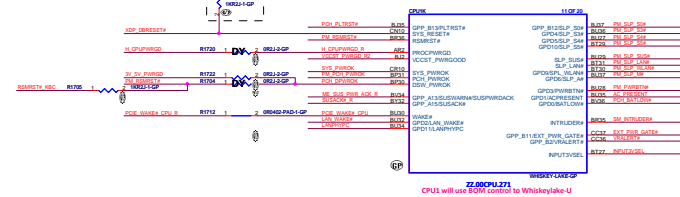
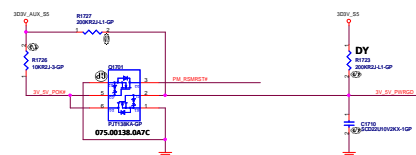
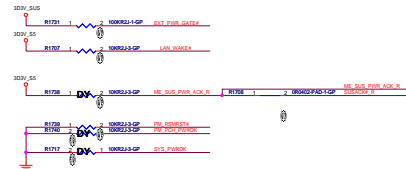
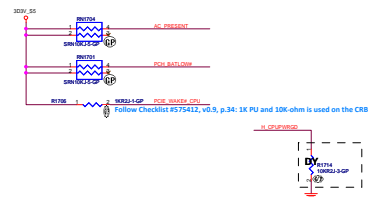
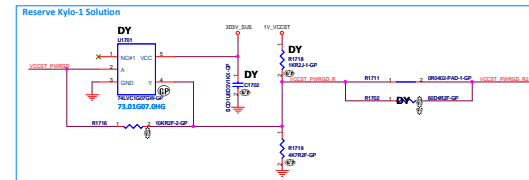
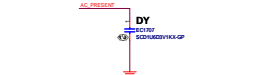
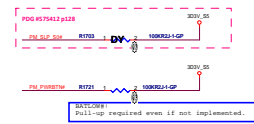
2. Trace Width: 4 mils min (breakout) 12-15 mils (trace)  
Note: Must maintain low DC resistance routing ( $<0.1 \Omega$ )  
2. Isolation Spacing: At least 12 mils to any adjacent

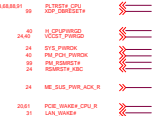
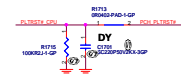
USB3.0 Configuration			Premium-WHL-U			Base-WHL-U		
Pair 1 Device		Pair 2 Device	Pair 1 Device		Pair 2 Device	Pair 1 Device		Pair 2 Device
PCIe Configuration			PCIe Configuration			PCIe Configuration		
1	USB3 Type-C Port1	1	1	USB3 Type-C Port1	1	1	USB3 Type-C Port1	1
2	USB3 Type-C Port2	2	2	USB3 Type-C Port2	2	2	USB3 Type-C Port2	2
3	USB3 Type-A Port1	3	3	USB3 Type-A Port1	3	3	USB3 Type-A Port1	3
4	USB3 Type-A Port2	4	4	USB3 Type-A Port2	4	4	USB3 Type-A Port2	4
5	NC	5	5	RGB	5	5	RGB	5
6	NC	6	6	Touch Screen	6	6	Touch Screen	6
7	NC	7	7	ImageLight	7	7	ImageLight (N/A)	7
8	NC	8	8	IR Camera	8	8	IR Camera	8
9	NC	9	9	World Facing Camera	9	9	World Facing Camera	9
10	WLAN	10	10	Bluetooth (N/A)	10	10	Bluetooth (N/A)	10
11	M.2 PCIe SSD							
12	M.2 PCIe SSD							
13	M.2 PCIe SSD							
14	M.2 PCIe SSD							
15	Media Card Reader							
16	NC							
17	NC							
18	NC							
19	NC							

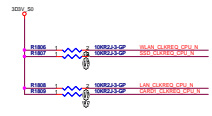
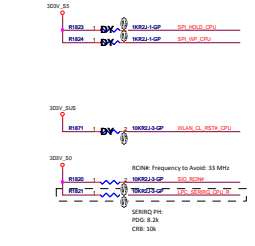
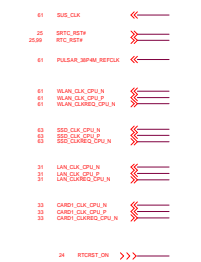
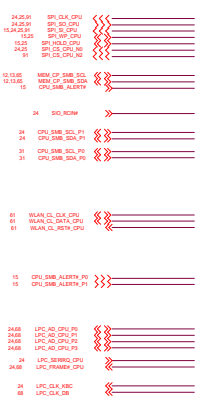




R12\_SVT\_ASR\_W0009


 R12\_SVT\_ASR\_W0009  
 R12\_SVT\_ASR\_W0009

 R12\_SVT\_ASR\_W0009  
 R12\_SVT\_ASR\_W0009

 R12\_SVT\_ASR\_W0009  
 R12\_SVT\_ASR\_W0009


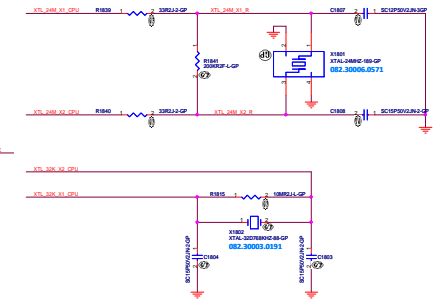
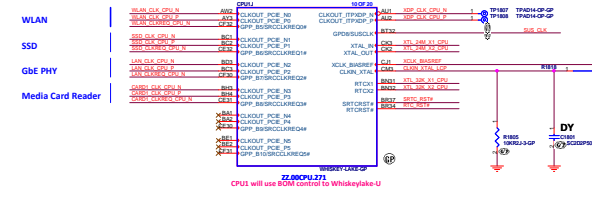
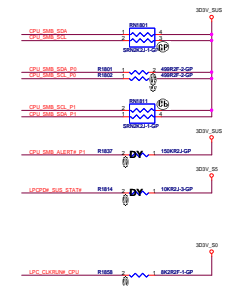
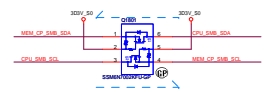
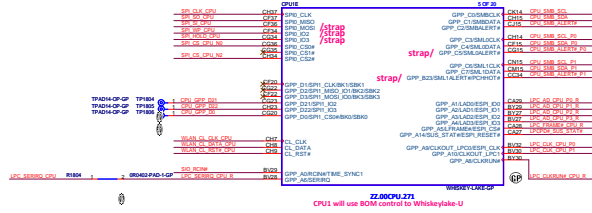


PCH strap pin: SPI_X0_CPU	
BOOT_HALT	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

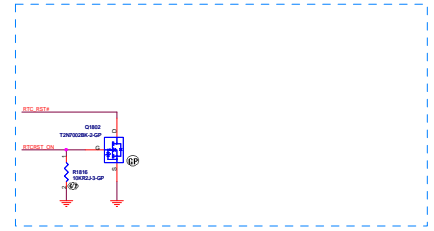
PCH strap pin: CPU_SMB_ALERTN_P0	
eSPI or LPC	Sampled at rising edge of RSMRSTR
SMBALERTN / GPP_CS	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

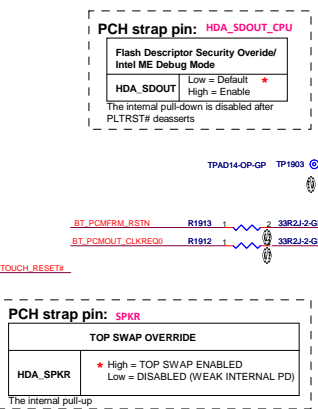
This signal has a weak internal pull-down.



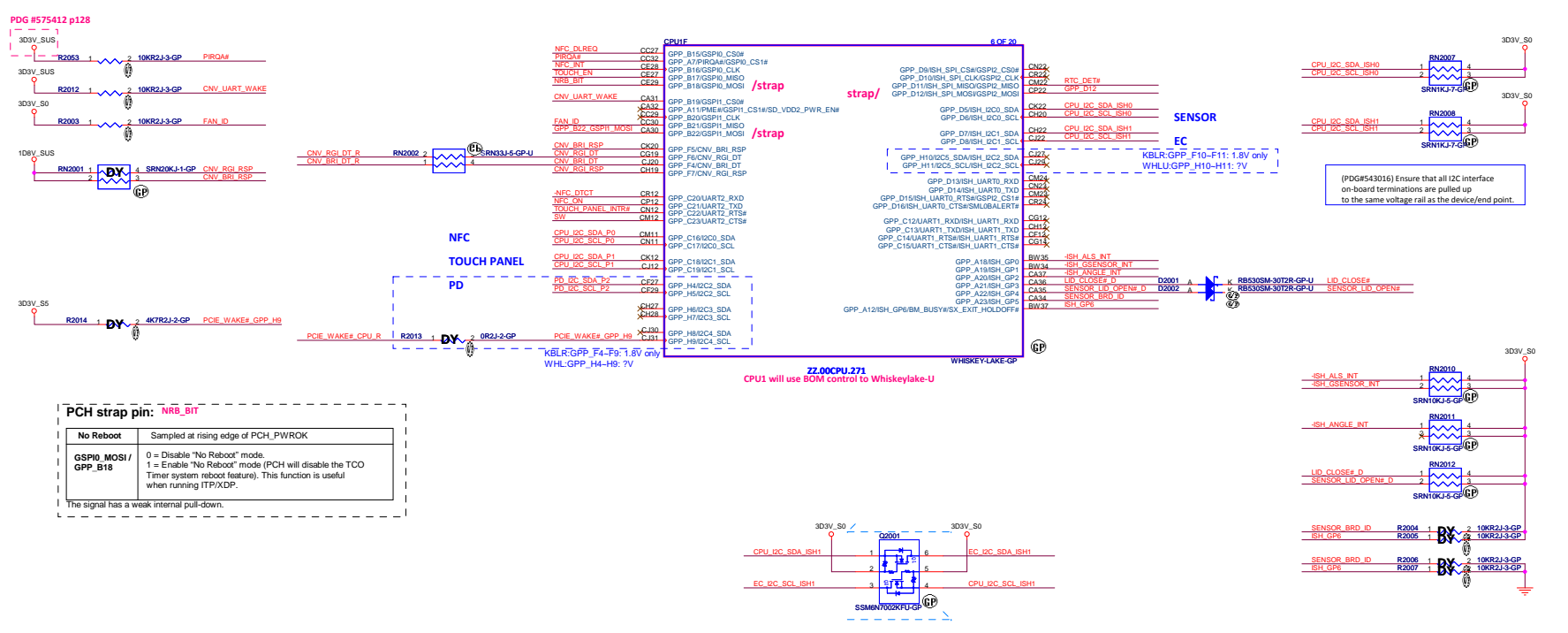
24MHz (X1801)  
TVC 7V24000023 082.30006.0171  
HARMONY X50204000C18A-HU 082.30006.0131

32.768KHz (X1802)  
EPSON EF-FC-135R 32.768K12.5+-20 (X1A000141000100) 082.30003.0191  
SEIKO Q-3C32P03220C3AAAF 082.30003.0001  
TVC W003200042 082.30003.0231



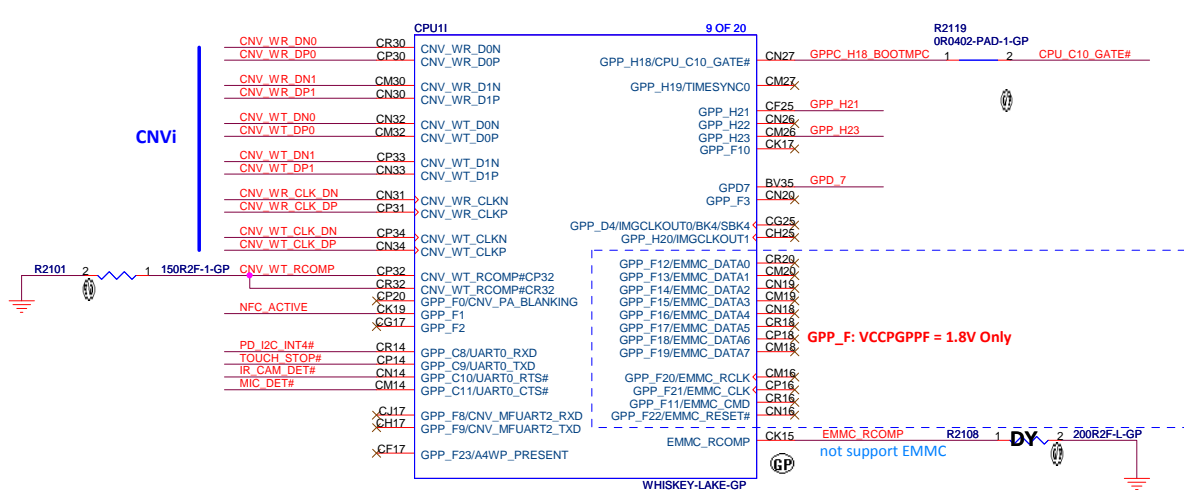
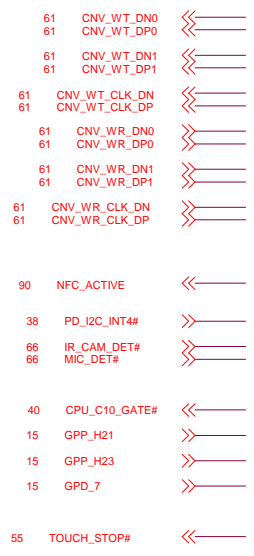


## KL2 SIT MB W016

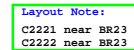


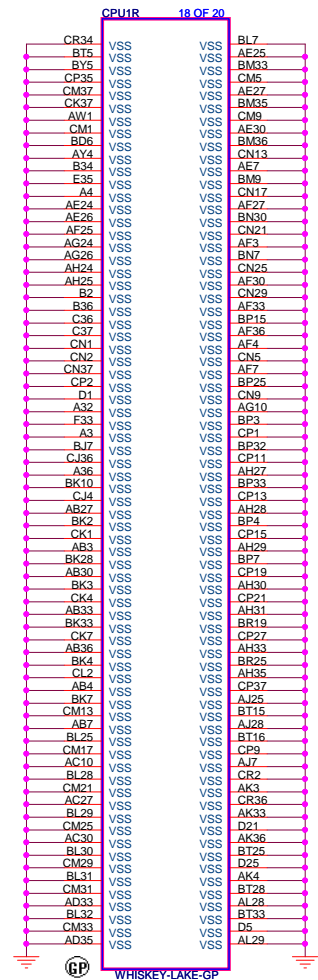
Main Func = PCH

CNVi

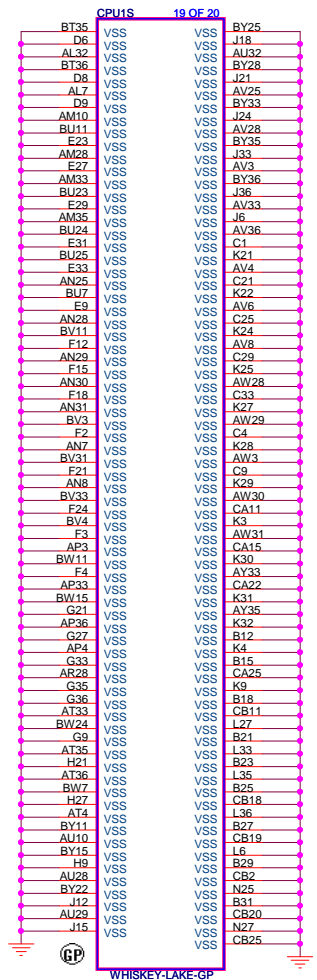


ZZ.00CPU.271  
CPU1 will use BOM control to Whiskeylake-U

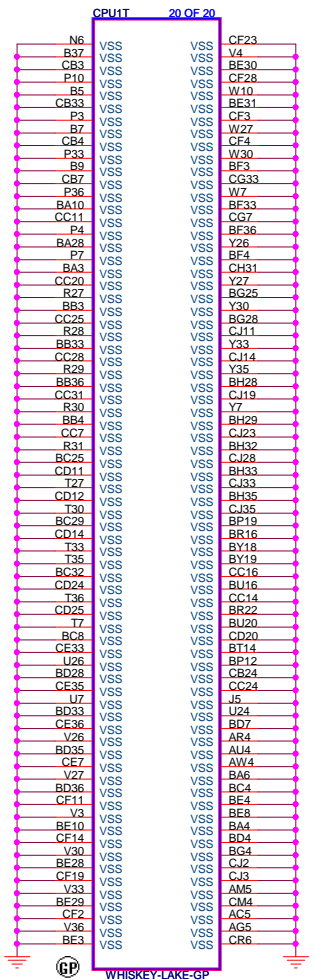




CPU1 will use BOM control to Whiskeylake-U

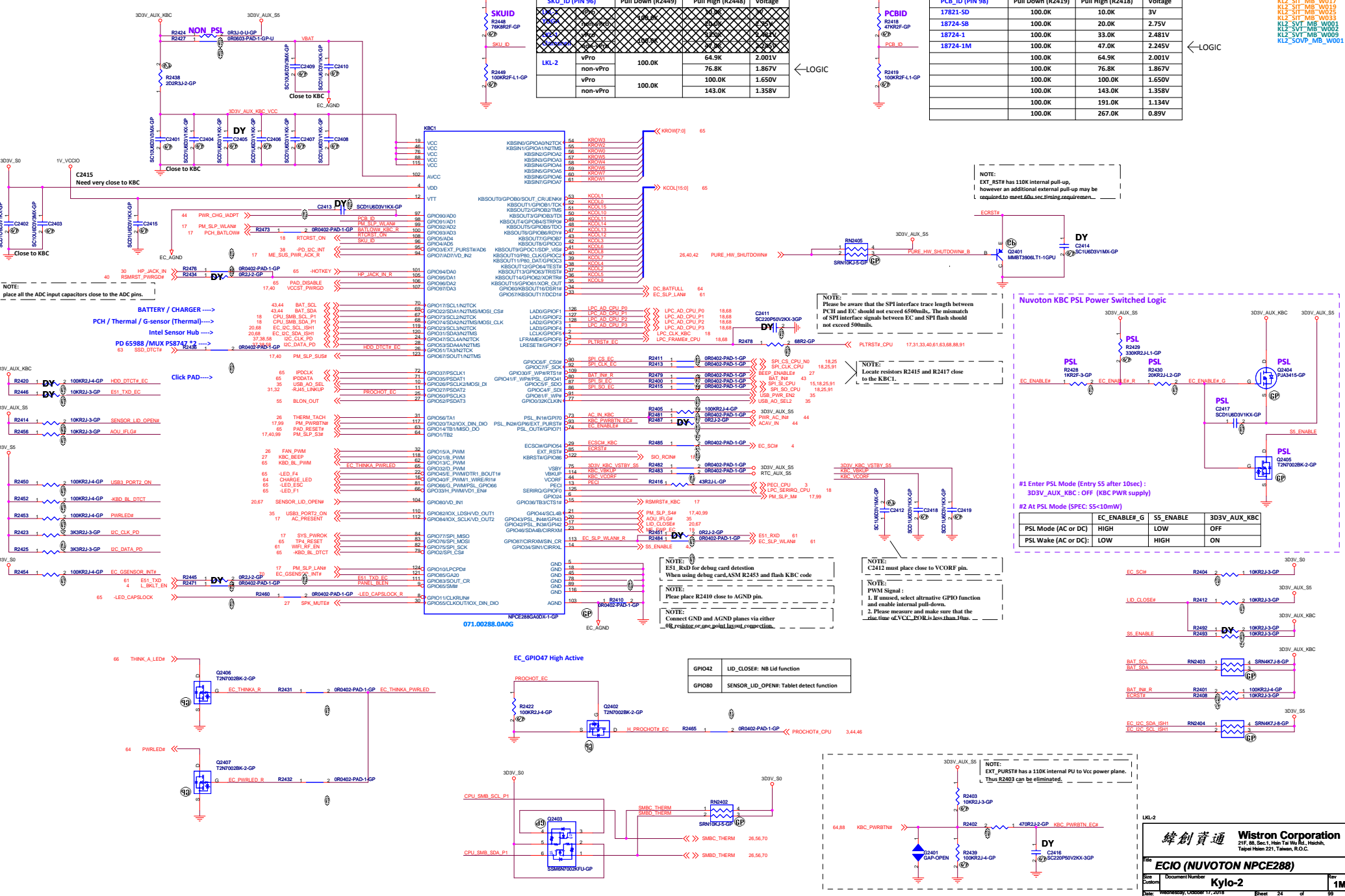


CPU1 will use BOM control to Whiskeylake-U



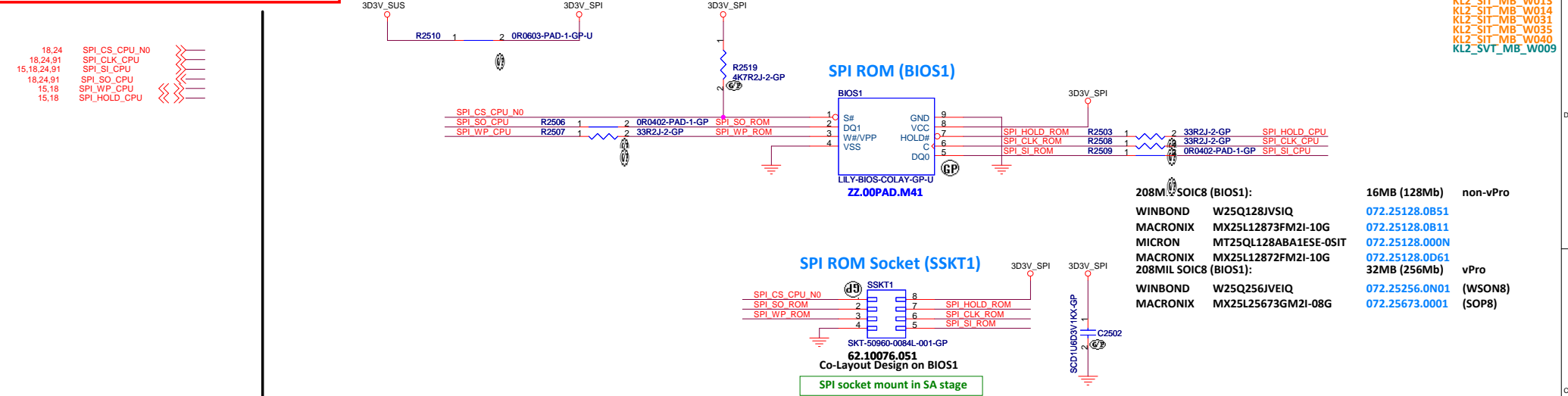
CPU1 will use BOM control to Whiskeylake-U

Main Func = KBC

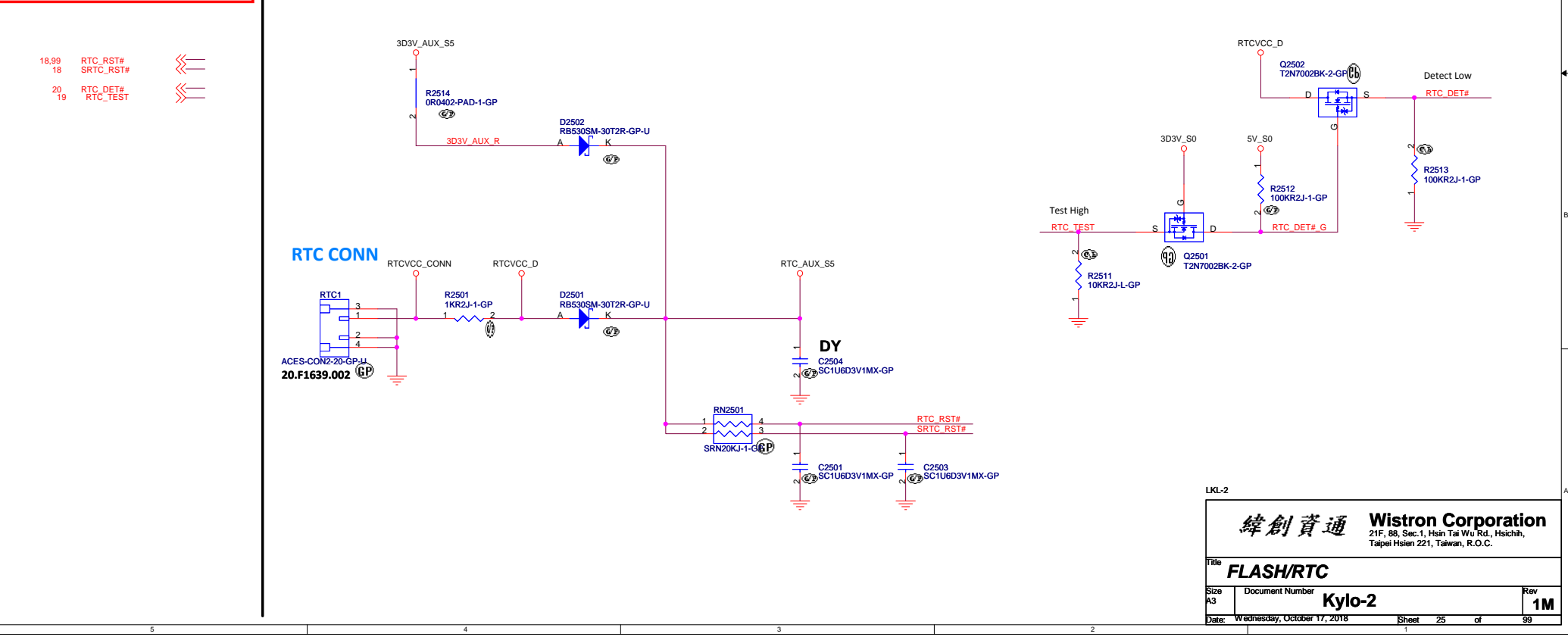




Main Func = SPI Flash



Main Func = RTC



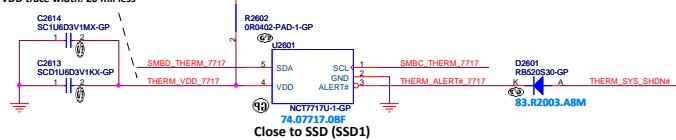
Thermal Sensor



CPU backside or inside the socket

CPU TEMP:  
H\_THERMDA and H\_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

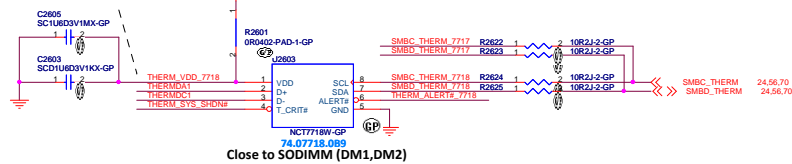
Layout NOTE:  
VDD trace width: 20 mil less



FAN Controller

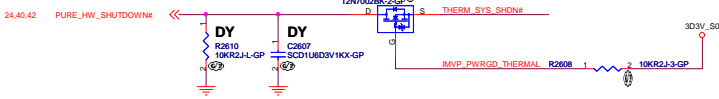
NCT7717U's maximum power consumption can be xxx mA (TBD)  
NCT7718W's maximum power consumption can be xxx mA (TBD)

Layout NOTE:  
VDD trace width: 20 mil less



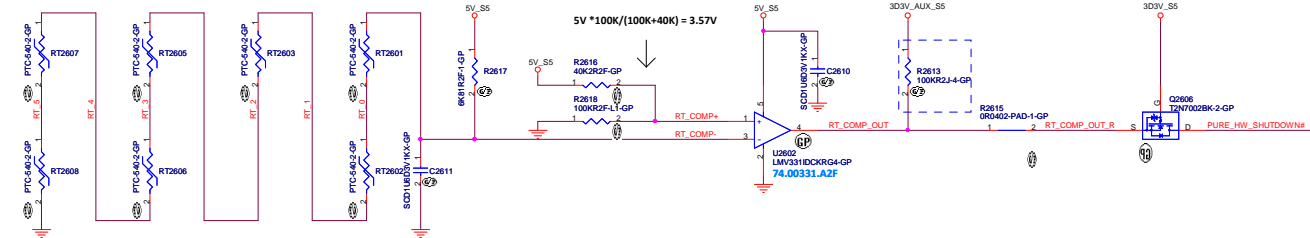
ALERT# / T\_CRIT# Pull-up Resistor v.s. Alert temperature (°C)

NCT7717U Table:		NCT7718W Table:							
R2619		R2621	2.0K	7.5K	10.5K	14.0K	18.7K		
2.0K	75	2.0K	77	87	97	107	117		
7.5K	90	7.5K	79	89	99	109	119		
10.5K	100	10.5K	81	91	101	111	121		
14.0K	105	14.0K	83	93	103	113	123		
18.7K	110	18.7K	85	95	105	115	125		



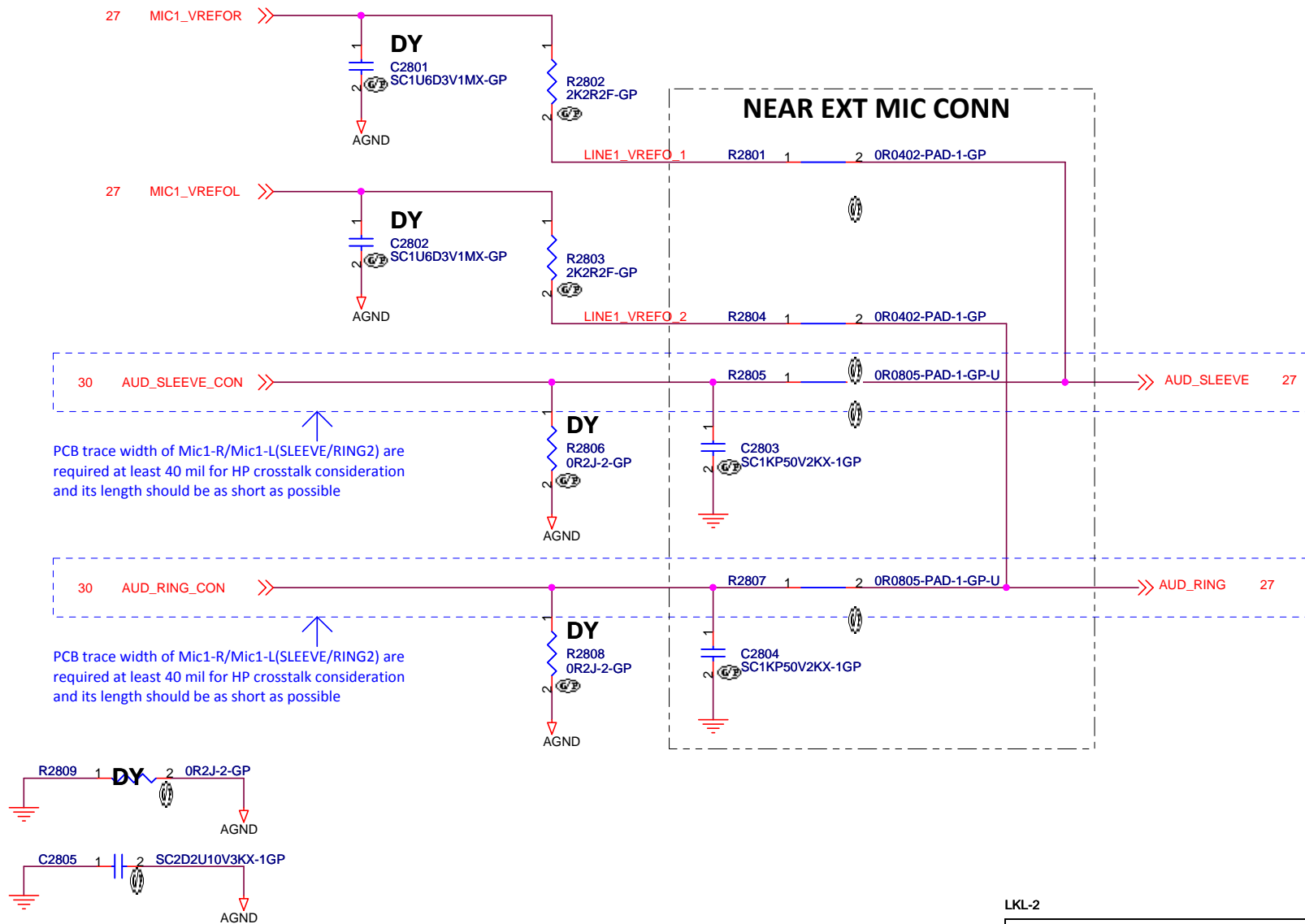
PURE\_HW\_SHUTDOWN# logic table

signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low



LKL-2





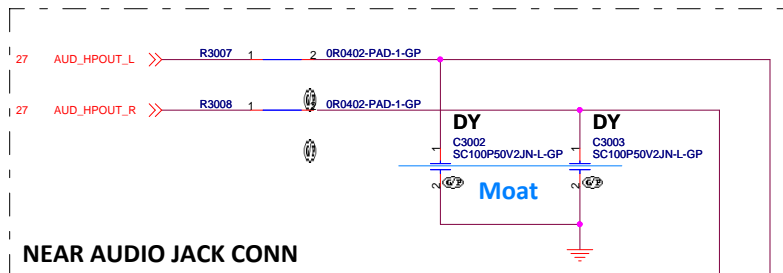
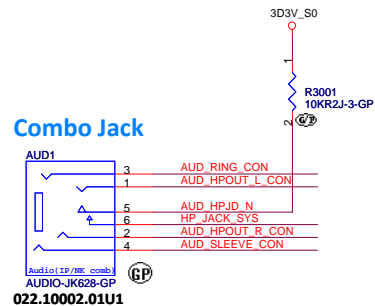
LKL-2

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.Title  
**AUDIO (MIC I/F)**Size A4 Document Number **Kylo-2** Rev **1M**

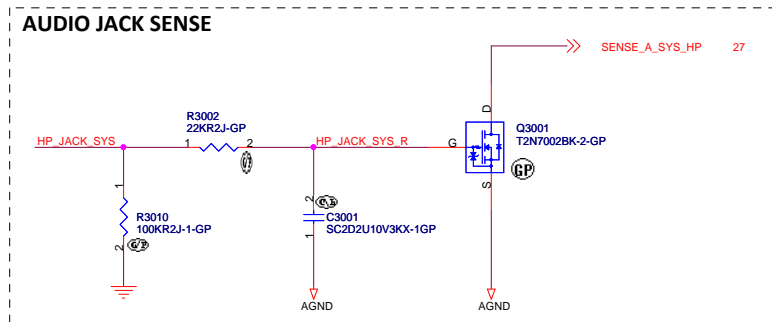
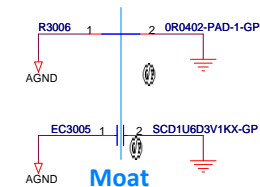
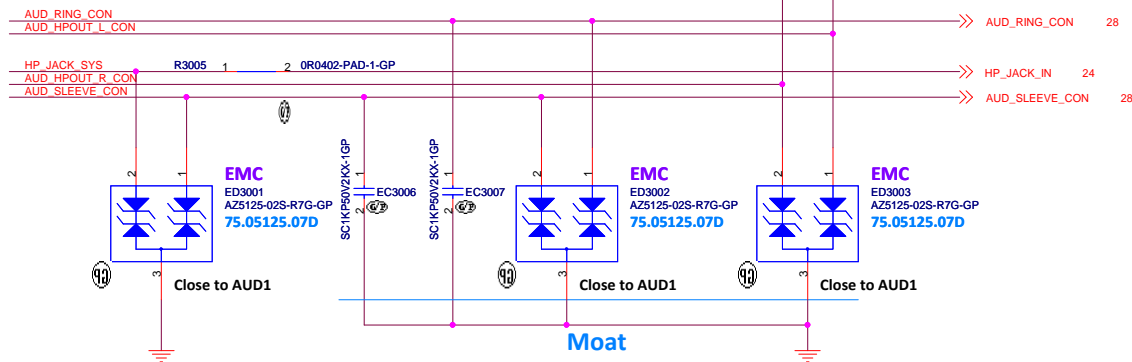
Date: Wednesday, October 17, 2018 Sheet 28 of 99





**AUDIO JACK SENSE**  
CLOSE TO CODEC  
6-10 mil trace recommend

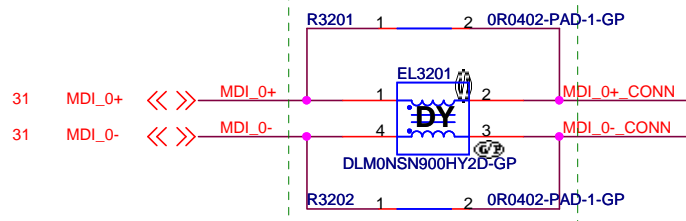
HGND A/HGND B trace width >70mil,  
changed to sharp will be better.



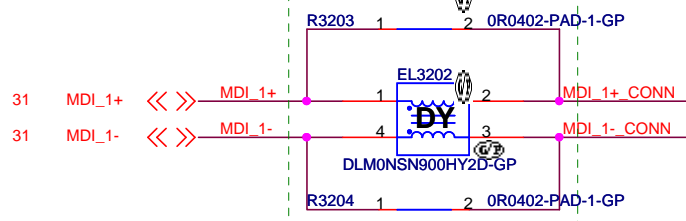
LKL-2

Date: Wednesday, October 17, 2018 Sheet 31 of 99

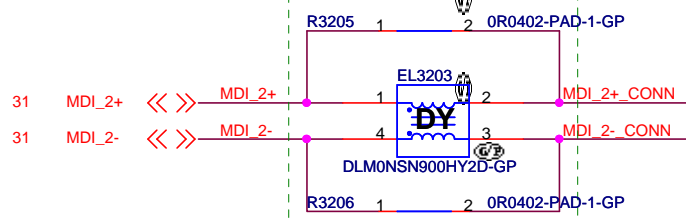
### Dual Layout



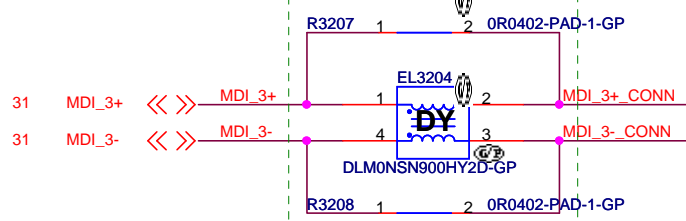
### Dual Layout



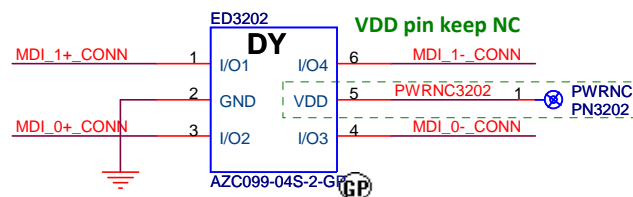
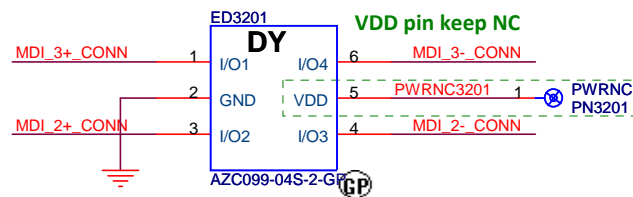
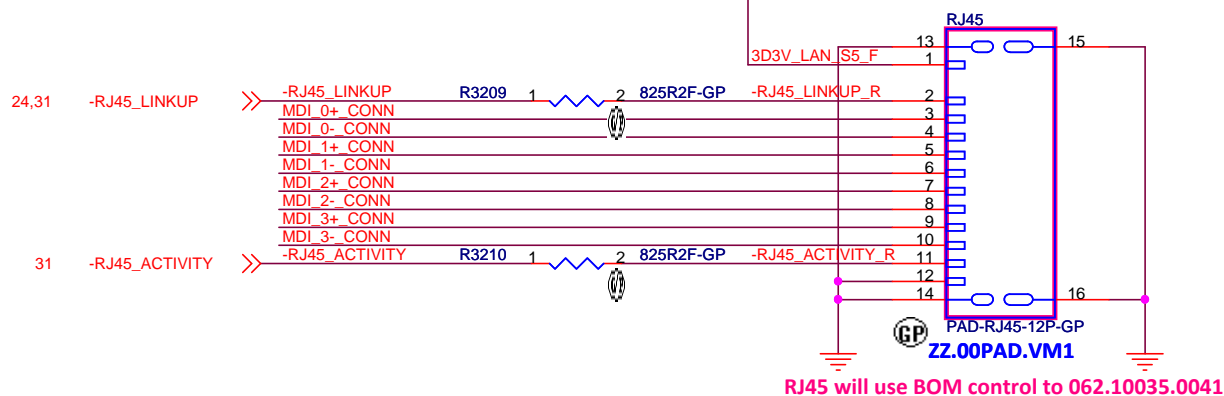
### Dual Layout



### Dual Layout



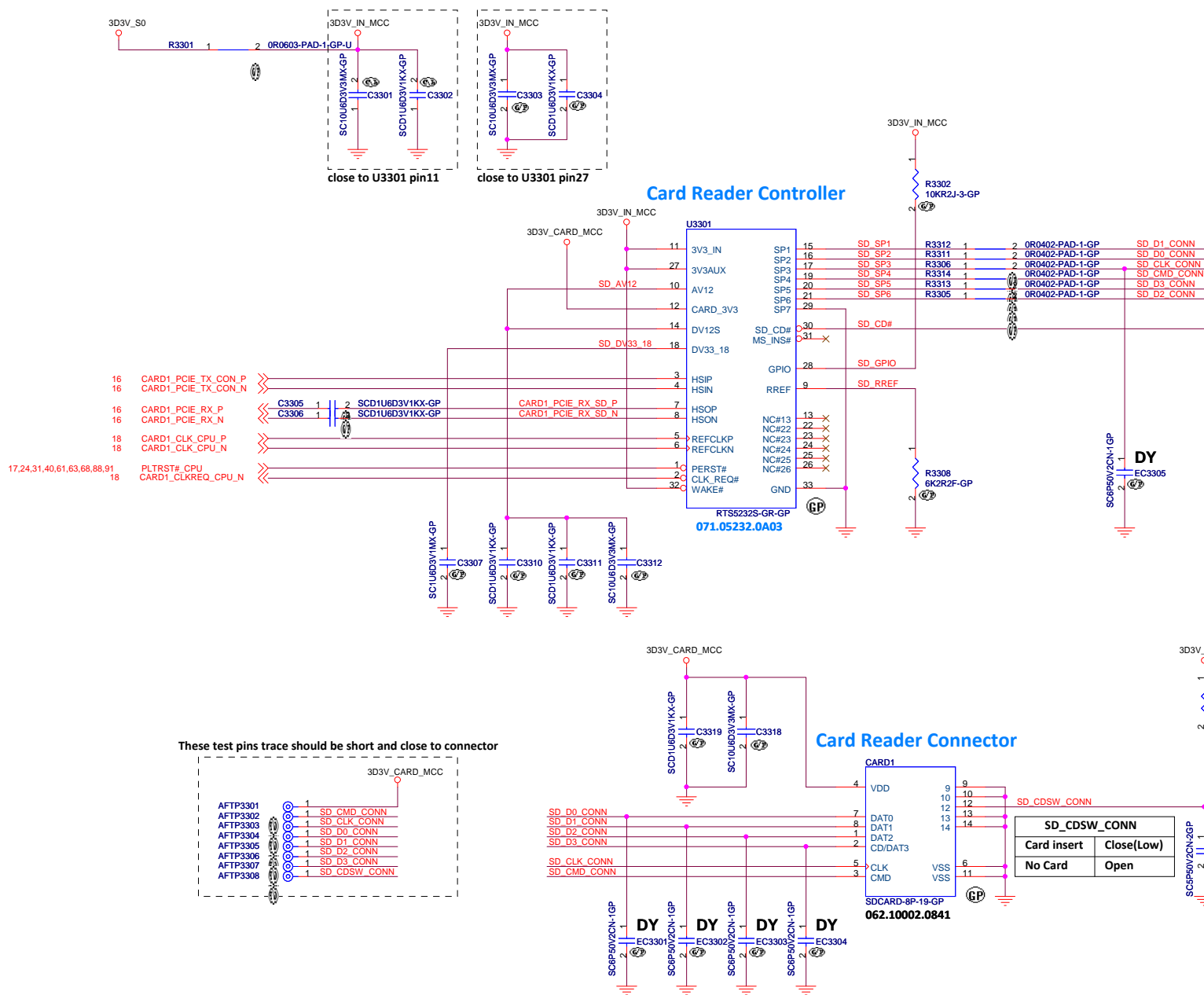
### UNIQUE RJ45 CONN (RJ45)



LKL-2

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title LAN (GBE DONGLE I/F)			
Size A4	Document Number	Kylo-2	Rev 1M
Date: Wednesday, October 17, 2018	Sheet 32	of 99	



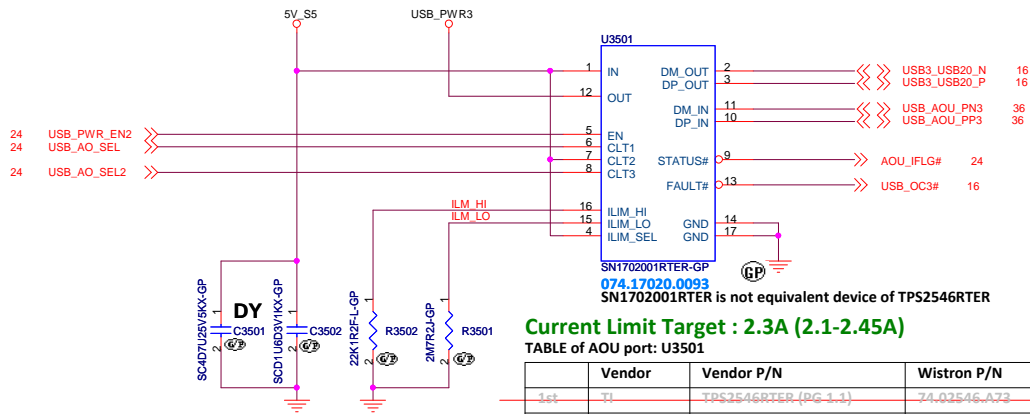


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LKL-2

<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <b>USB (RSVD)</b>		
Size A4	Document Number <b>Kylo-2</b>	Rev <b>1M</b>
Date: Wednesday, October 17, 2018		Sheet 34 of 99

For USB3.0 System Port3 (For AOU)



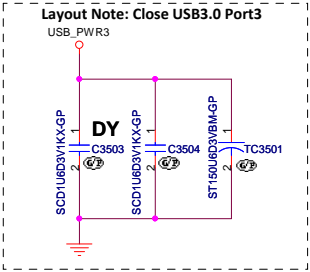
Current Limit Target : 2.3A (2.1-2.45A)

TABLE of AOU port: U3501

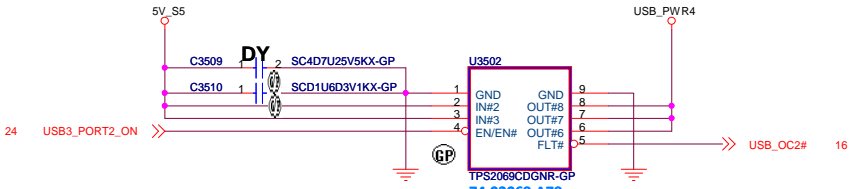
	Vendor	Vendor P/N	Wistron P/N
1st	TI	TPS2546RTER (PG 1.1)	74.02546.A73
1st	TI	SN1702001RTER (PG 1.1)	074.17020.0093
2nd	Pericom	PI5USB2546ZHEX-REV.X	074.52546.0A73
2nd	DIODES	PI5USB2546HZHEX	074.52546.0D73

(had iPhone 6/7 charging issue)

(had iPhone 6/7 charging issue)



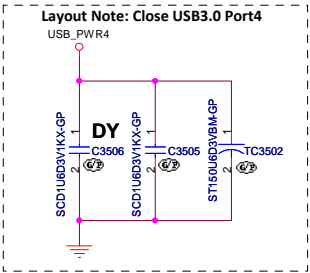
For USB3.0 System Port4



Continous Current Limit 1.5A  
Non-Common Part

TABLE of USB 3.0 port: U3502

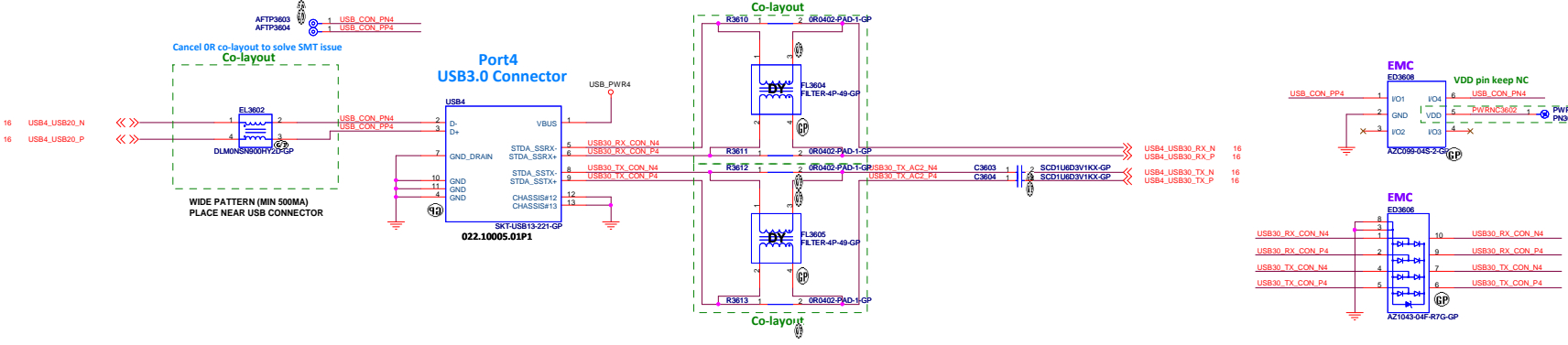
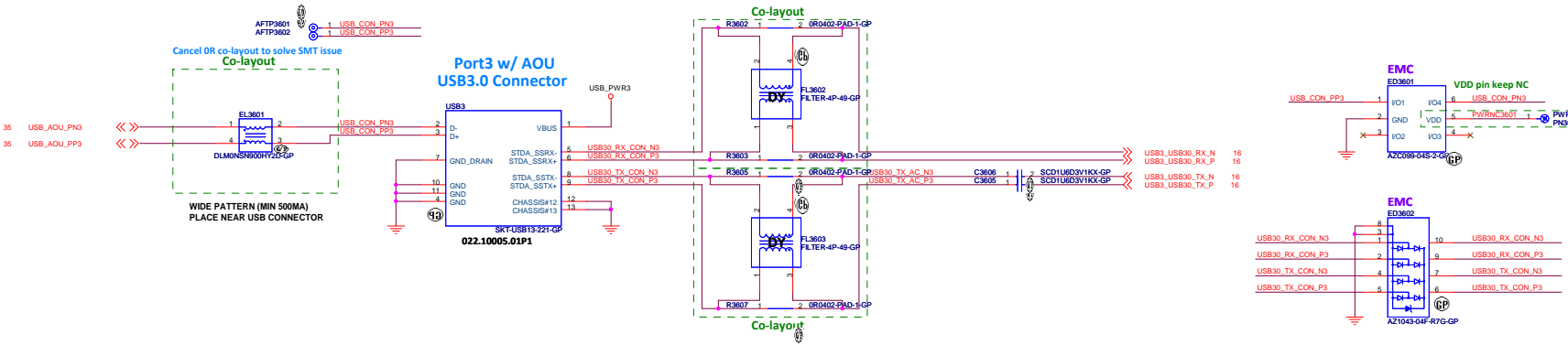
	Vendor	Vendor P/N	Wistron P/N
1st	TI	TPS2069CDGMR	74.02069.A79
2nd	ROHM	BD82032FVJ-GE2	74.82032.07G

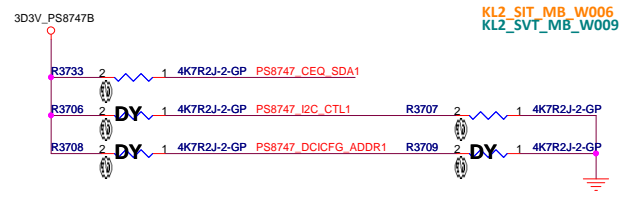
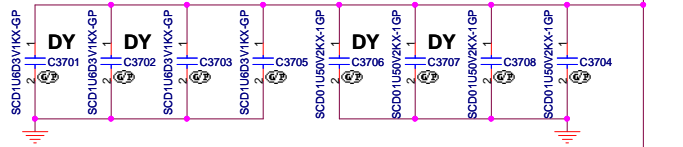
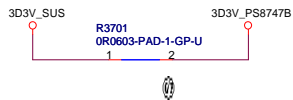


LKL-2

Main Func = USB3.0 Port3 w/ AOU  
Main Func = USB3.0 Port4

KL2\_SIT\_MB\_W006  
KL2\_SIT\_MB\_W022  
KL2\_SVT\_MB\_W009  
KL2\_SVT\_MB\_W010



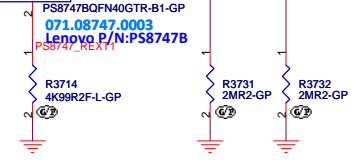
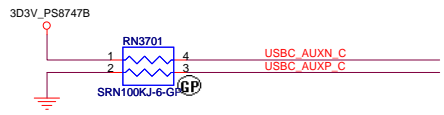
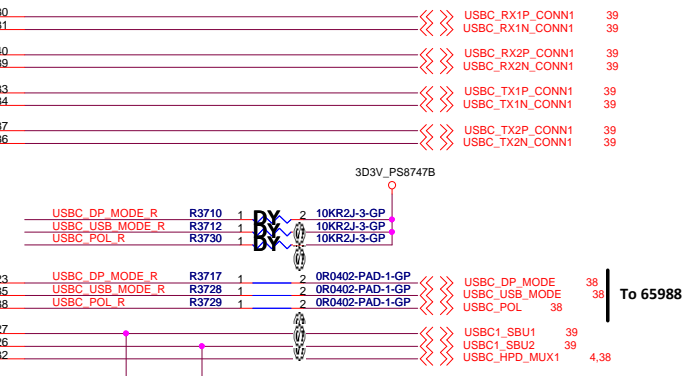
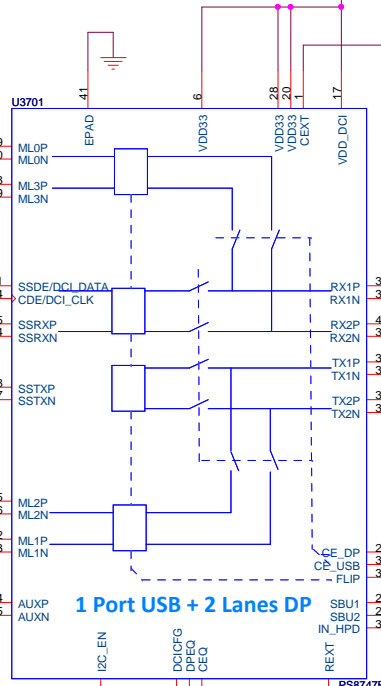
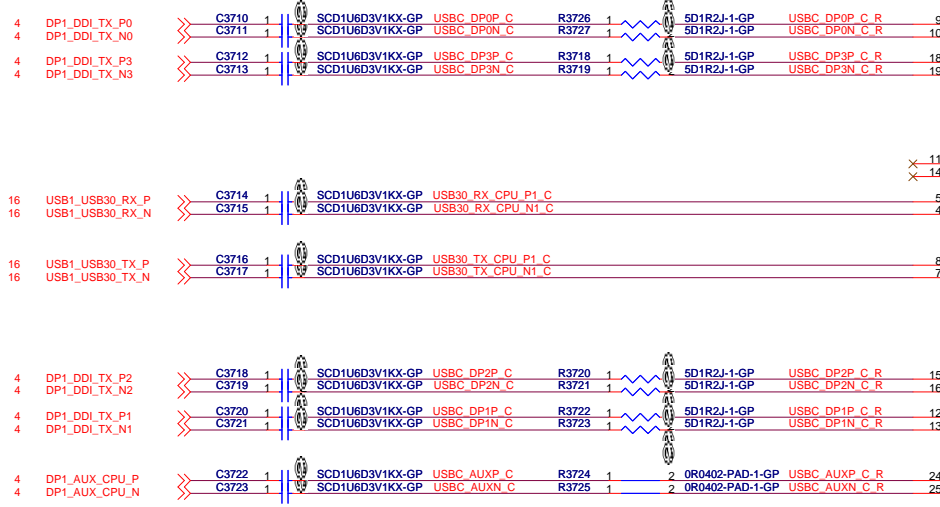


PS8747_I2C_CTL1 =	
L: Pin Control is selected	R3706: DY, R3707: ASM
H: I2C Control is selected	R3706: ASM, R3707: DY

-- LOGIC

PS8747_DCICFG_ADDR1 =	
(Pin Control mode only) =	
L: DCI mode disabled	R3708: DY, R3709: ASM
H: DCI mode enabled	R3708: ASM, R3709: DY
M: Automatic DCI mode entering enabled	R3708: DY, R3709: DY
(I2C Control mode only) =	
L: 0x20/0x21 (Default)	R3708: DY, R3709: ASM
H: 0x22/0x23	R3708: ASM, R3709: DY

-- LOGIC



緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **USB (TYPEC MUX PS8747B)**

Size A3 Document Number **Kylo-2** Rev **1M**

Date: Wednesday, October 17, 2018 Sheet 37 of 99







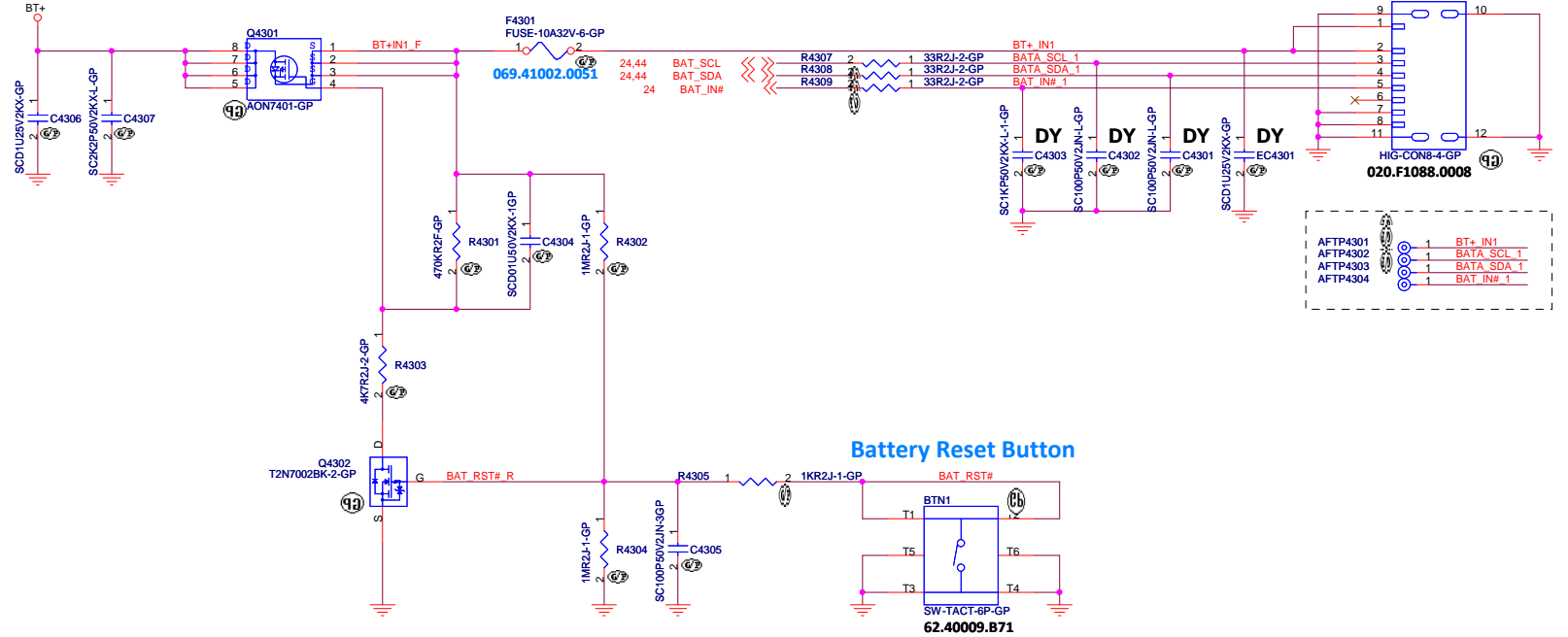


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LKL-2

<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <b>SEQUENCE (RSVD)</b>		
Size A4	Document Number <b>Kylo-2</b>	Rev <b>1M</b>
Date: Wednesday, October 17, 2018		Sheet 41 of 99





LKL-2

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title  
**INT IO (BATT CONN)**

Size A3 Document Number **Kylo-2** Rev **1M**

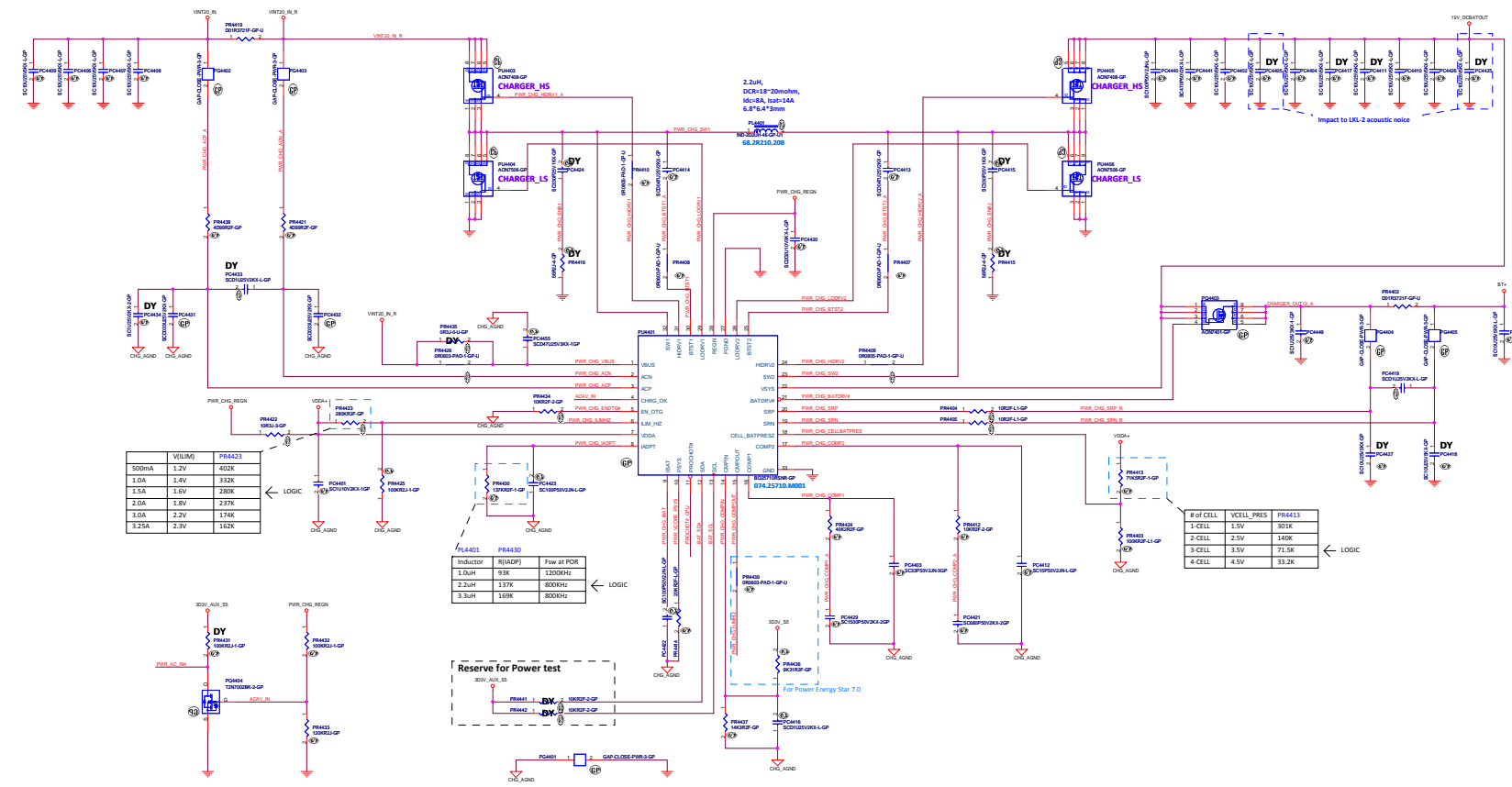
Date: Wednesday, October 17, 2018 Sheet 43 of 99

## OFFPAGE

PH on EE Side



PH on EE Side



	V(IUM)	PR4423
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

Inductor	R(IADP)	Fsw at POR
1.0uH	93K	1200KHz
2.2uH	137K	800KHz
3.3uH	169K	800KHz

# of CELL	VCELL_PRES	PR4413
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

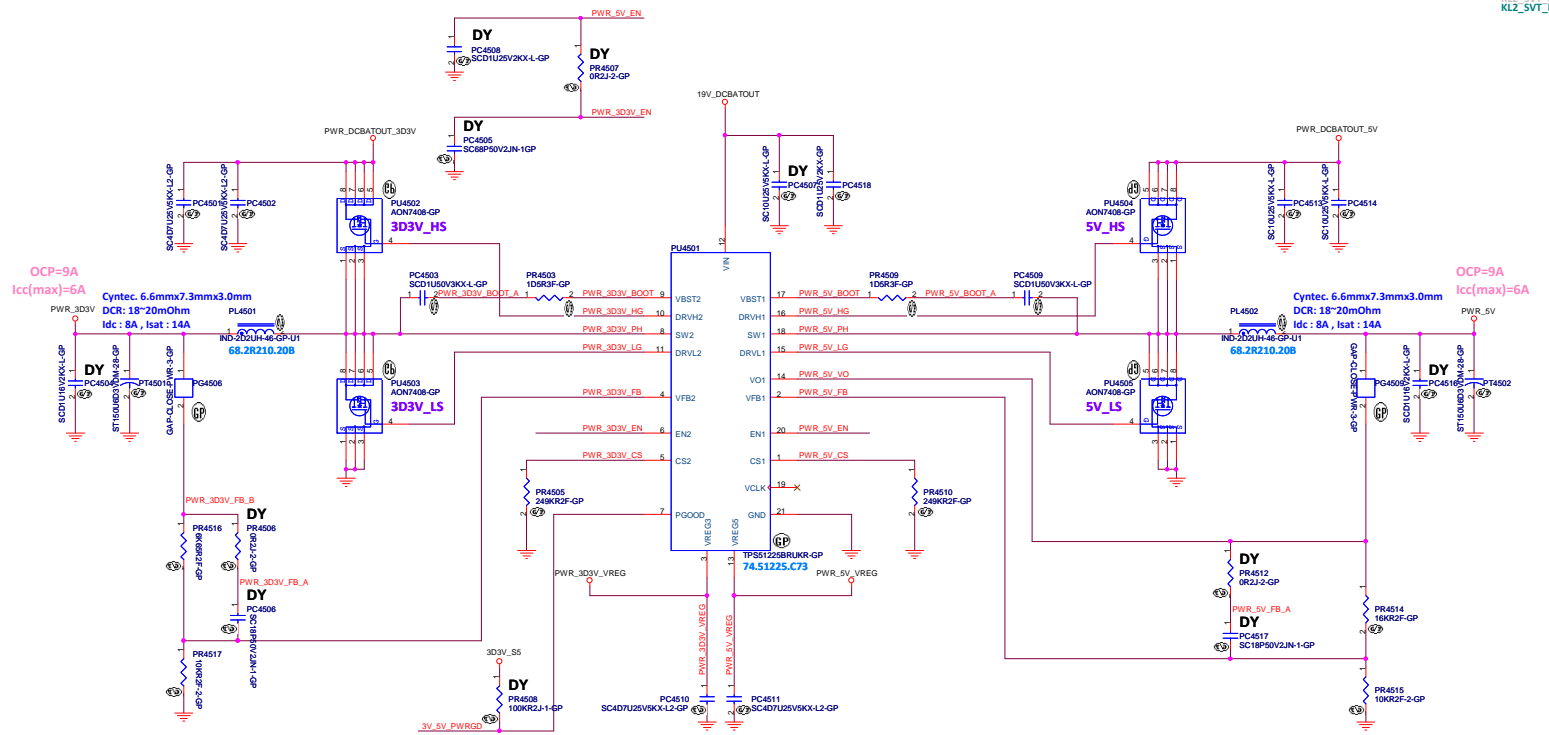
LWL-2

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,

File	<b>POWER (CHARGER_BQ25710RSNR)</b>	
Doc A1	Document Number <b>Kylo-2</b>	Rev <b>1M</b>

Page A-1	Kylo-2	Date 1M
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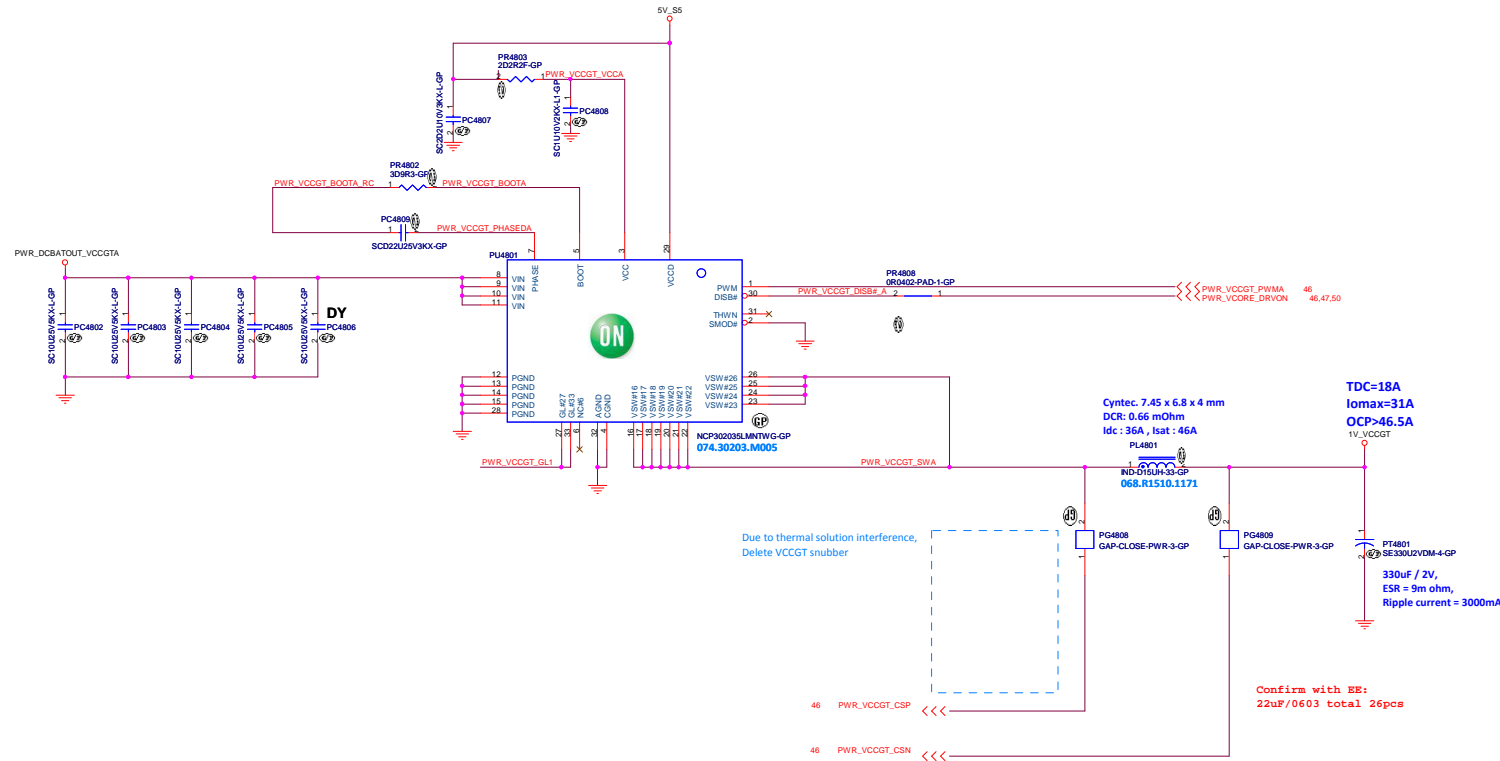
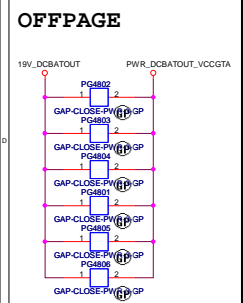
KL2\_SIT\_MB\_W009  
KL2\_SIT\_MB\_W021  
~~KL2\_SVT\_MB\_W004~~  
KL2\_SVT\_MB\_W007



### PH on CPU side







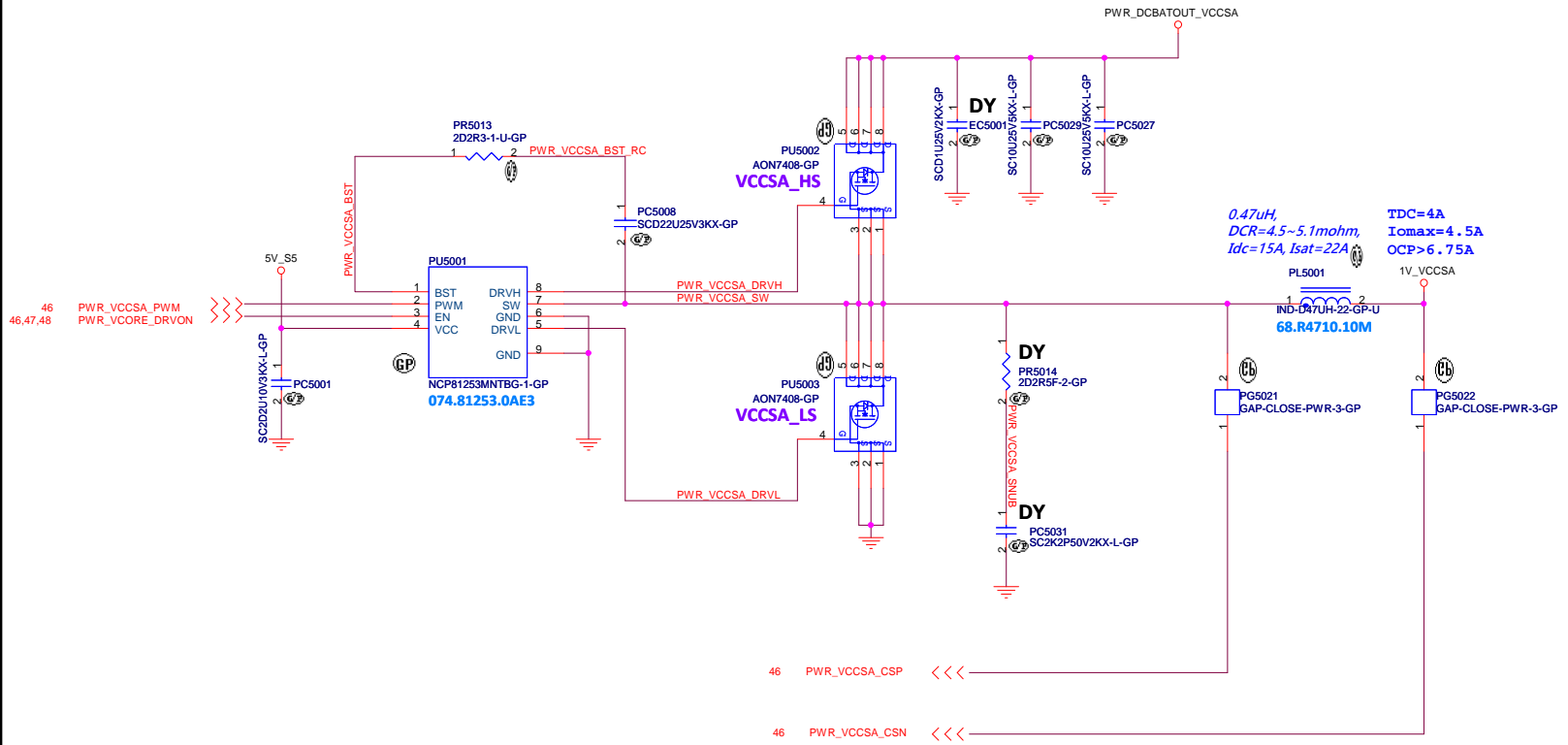


Main Func = CPU\_CORE

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LKL-2

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <b>POWER (RSVD)</b>		
Size A4	Document Number <b>Kylo-2</b>	Rev <b>1M</b>
Date: Wednesday, October 17, 2018		
Sheet 49 of 99		



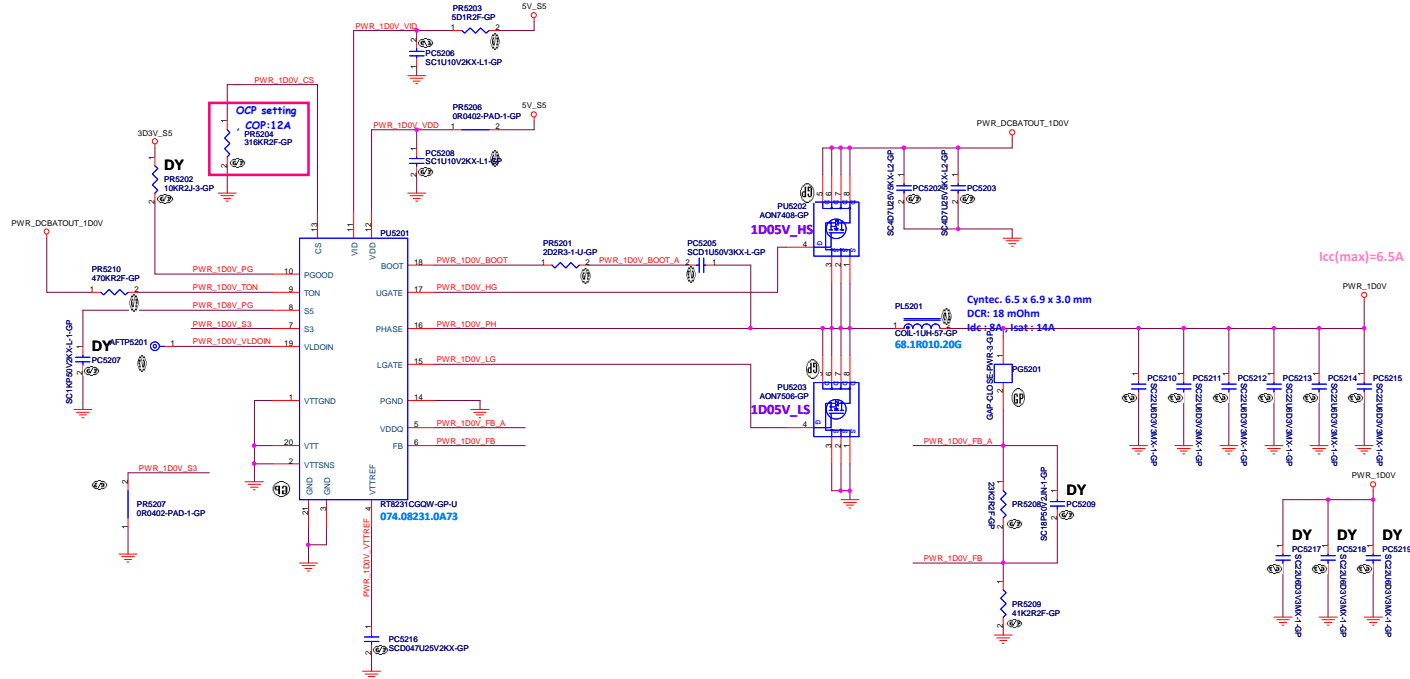
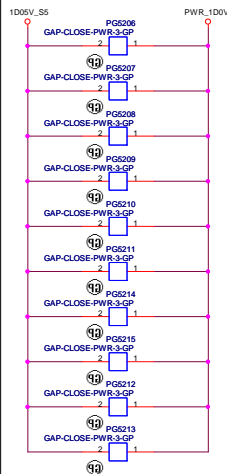
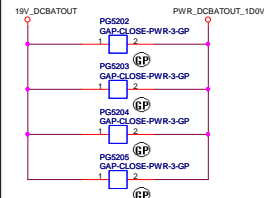
Size A2	Document Number <b>Kylo-2</b>	Rev <b>1M</b>
Date: Wednesday, October 17, 2018	Sheet 51 of 99	

# OFFPAGE

# OFFPAGE\_GAP

KL2\_SIT\_MB\_W021  
KL2\_SIT\_MB\_W024  
KL2\_SVT\_MB\_W007

PH on EE Side

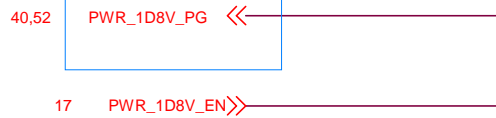


LKL-2

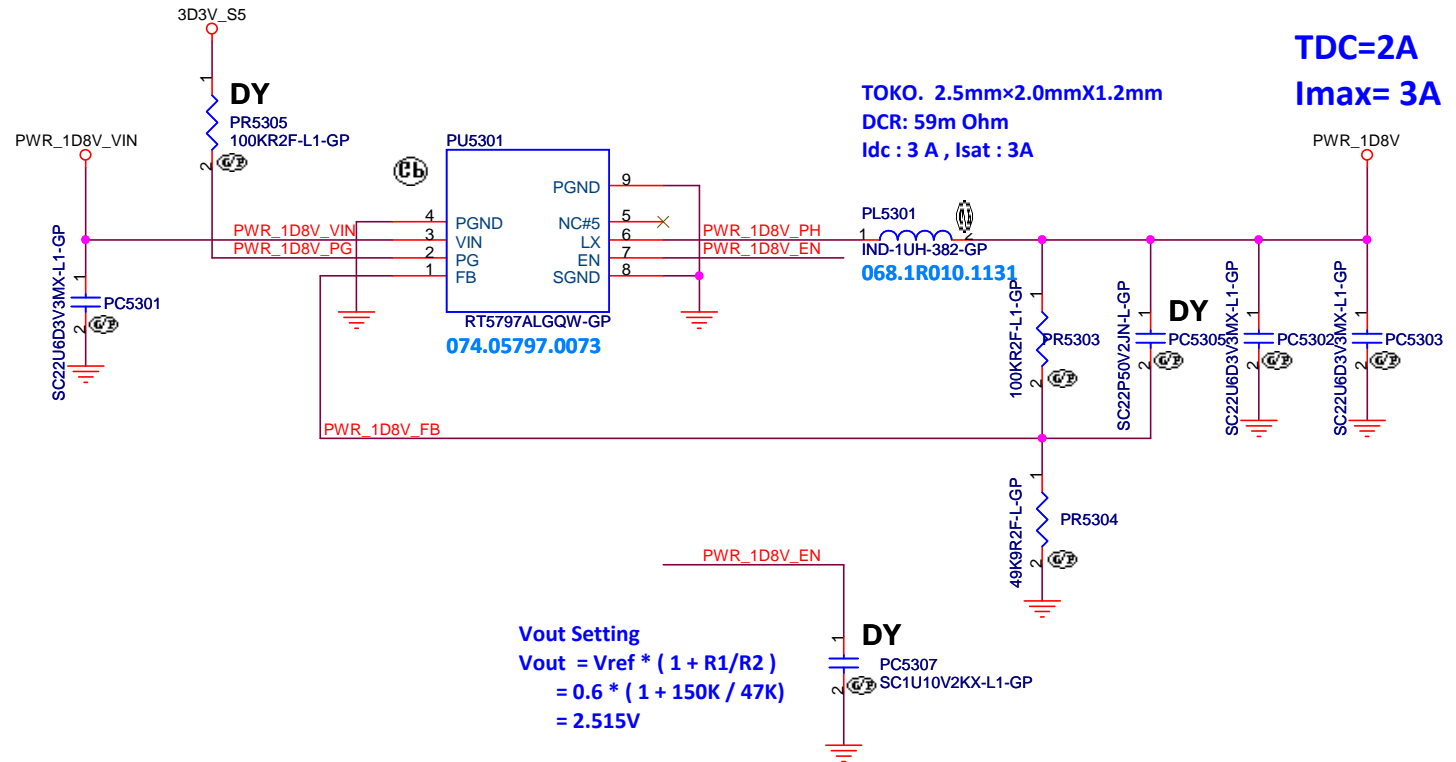
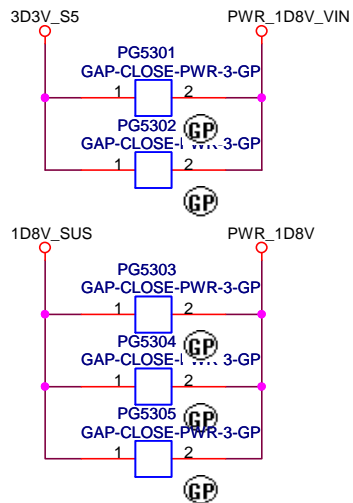
<b>緯創資通</b> Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File	<b>POWER (RT8231_1D05V)</b>
Size	Document Number
K2	<b>Kylo-2</b>
Date	Version
Wistron/Power/00000001/17_2018	1M
Sheet	62 of 99

# OFFPAGE

PH on EE Side



# OFFPAGE-GAP



LKL-2

<b>緯創資通</b> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>POWER (RT5797_1D8V)</b>	
Size A4	Document Number <b>Kylo-2</b>
Date: Wednesday, October 17, 2018	Sheet 53 of 99
Rev <b>1M</b>	

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LKL-2

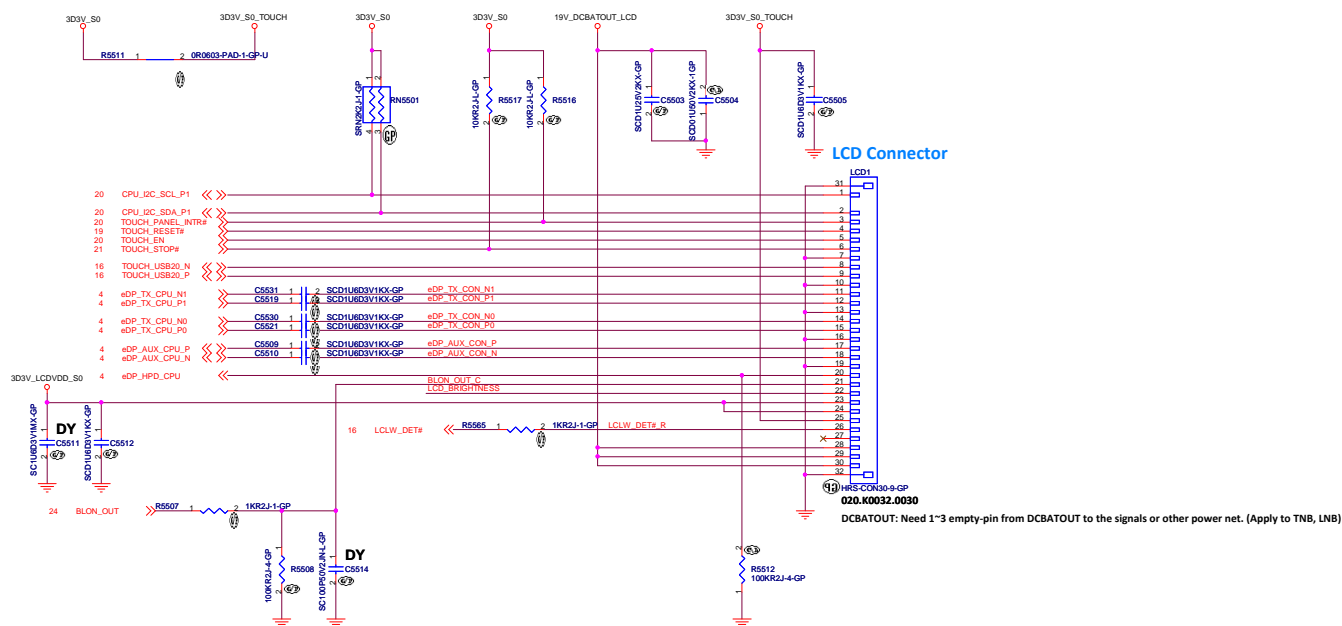
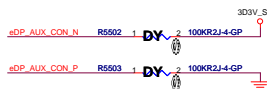
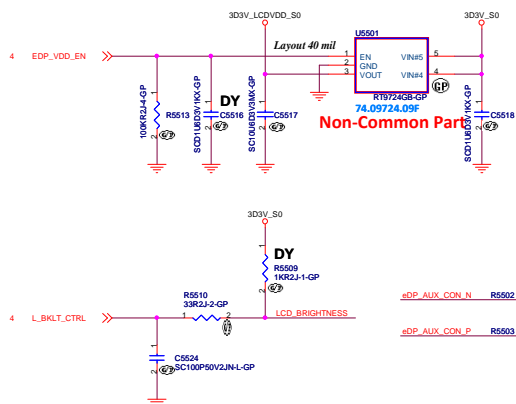
<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <b>POWER (RSVD)</b>		
Size A4	Document Number <b>Kylo-2</b>	Rev <b>1M</b>
Date: Wednesday, October 17, 2018	Sheet 54	of 99

Main Func = LCD

### LCD Backlight Power



**For LCD DCBATOUT inrush current**



**DCBATOUT:** Need 1~3 empty-pin from DCBATOUT to the signals or other power net. (Apply to TNB, LNB)

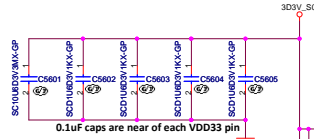
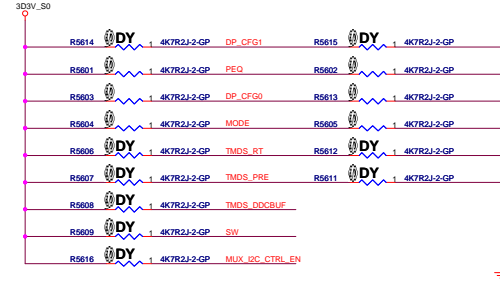
LKL-2

緯創資通 **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,

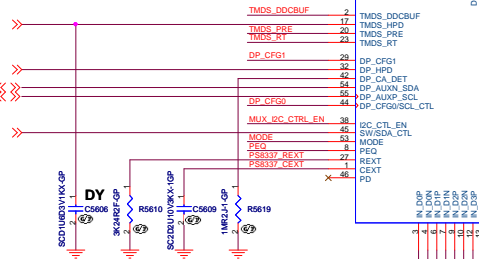
Title	<b>DISPLAY (LCD/CAM/TOUCH)</b>
-------	--------------------------------

Size A2	Document Number <b>Kylo-2</b>	Rev <b>1M</b>
Date: Wednesday, October 17, 2018	Sheet 55 of 99	

H: 4.7K-ohm  
M: 150K-ohm  
L: DY



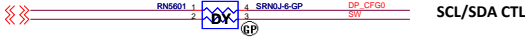
57.88 HDMI\_HPD\_CONN  
38.58 DP2\_HPD\_MUX  
58 USB2\_DP2\_AUXN  
58 USB2\_DP2\_AUXP  
20 SW



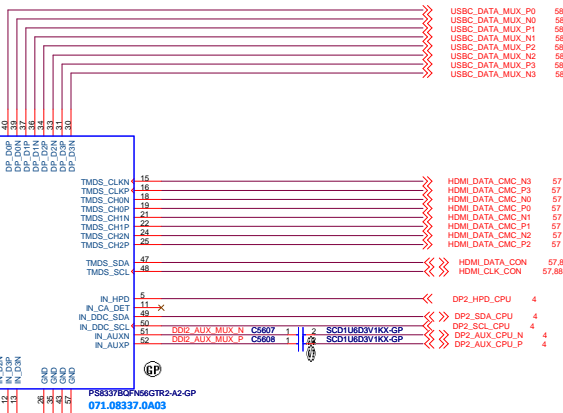
WHL DDI

4 DP2\_DDI\_TX\_P0  
4 DP2\_DDI\_TX\_N0  
4 DP2\_DDI\_TX\_P1  
4 DP2\_DDI\_TX\_N1  
4 DP2\_DDI\_TX\_P2  
4 DP2\_DDI\_TX\_N2  
4 DP2\_DDI\_TX\_P3  
4 DP2\_DDI\_TX\_N3

24.26.70 SMB2\_THERM  
24.26.70 SMB2\_THERM



SCL/SDA CTL



TYPE-C  
Priority first

HDMI

WHL DDI

TMD5\_PRE1 = L: no pre-emphasis  
= H: 1.50B pre-emphasis  
= M: 3.00B pre-emphasis  
The pin internal pull down at ~150K, 3.3V I/O.

TMD5\_RT1 = L: Standard open drain driver  
= H: Open drain driver with termination resistors  
The pin internal pull down at ~150K, 3.3V I/O.

TMD5\_DDCBUF1 = L: DDC pass through  
= H: DDC active buffer  
= M: DDC pass through with 40 kohm pull up resistor  
The pin internal pull down at ~150K, 3.3V I/O.

PEG1 = L: default, LEO, compensate channel loss up to 12dB @ HBR2  
= H: HEO, compensate channel loss up to 15dB @ HBR2  
= M: LLEO, compensate channel loss up to 5dB @ HBR2  
The pin internal pull down at ~150K, 3.3V I/O.

DP1\_CFG1 = L: default, auto test disable & input offset cancellation enable  
= H: auto test enable & input offset cancellation enable  
= M: auto test disable & input offset cancellation disable  
The pin internal pull down at ~150K, 3.3V I/O.

DP1\_CFG0 = L: default, automatic EQ enable & AUX interception enable  
= H: automatic EQ disable & AUX interception enable  
= M: automatic EQ disable, no pre-emphasis, 800mVpp swing  
The pin internal pull down at ~150K, 3.3V I/O.

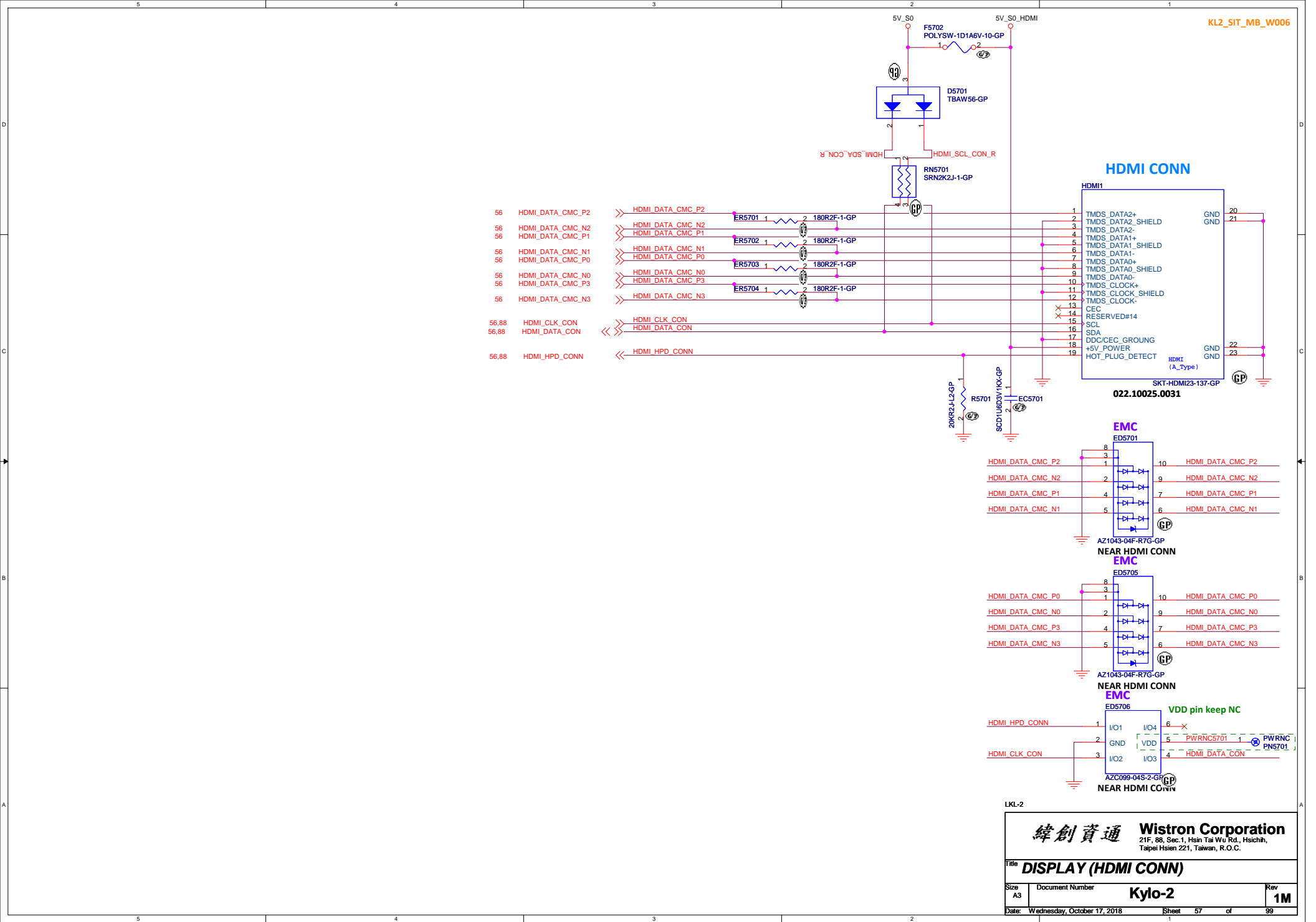
MODE1 = L: Control Switching Mode, HDMI ID disable  
= H: Automatic Switching Mode, HDMI ID disable  
= M: Automatic Switching Mode, HDMI ID enable  
The pin internal pull down at ~150K, 3.3V I/O.

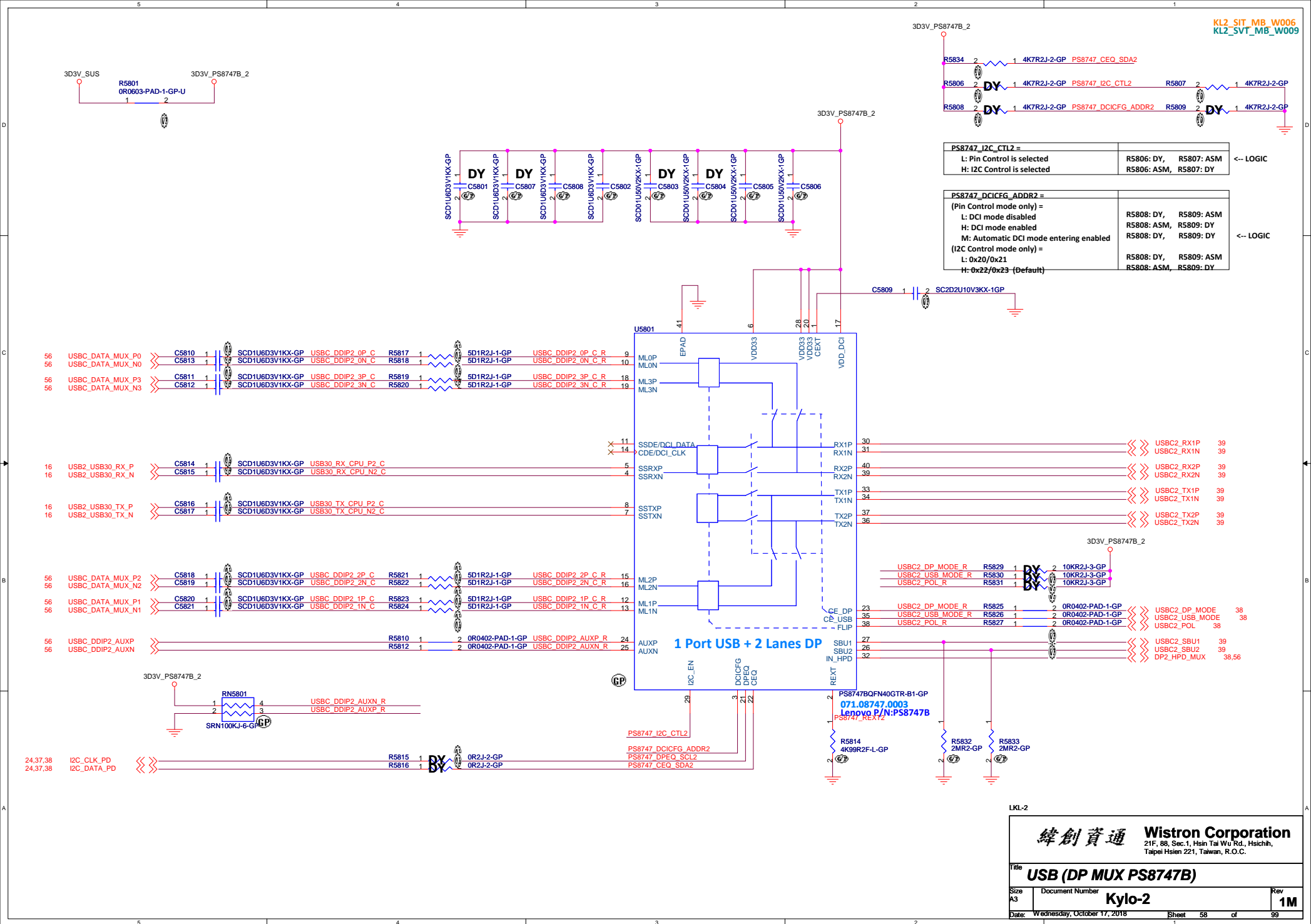
For Control Switching:  
SW 1= L: DP output is selected  
SW 1= H: TMD5 output is selected

For Automatic Switching:  
SW 1= L: DP output has higher priority  
The pin internal pull down at ~150K, 3.3V I/O.  
SW 1= H: TMD5 output has higher priority.

LKL-2







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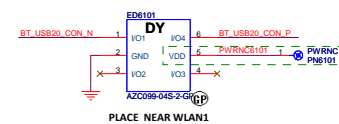
LKL-2

<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <b>DISPLAY (RSVD)</b>		
Size A4	Document Number <b>Kylo-2</b>	Rev <b>1M</b>
Date: Wednesday, October 17, 2018		Sheet 59 of 99

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LKL-2

<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <i><b>INT IO (RSVD)</b></i>		
Size A4	Document Number <b>Kylo-2</b>	Rev <b>1M</b>
Date: Wednesday, October 17, 2018		
Sheet 60 of 99		

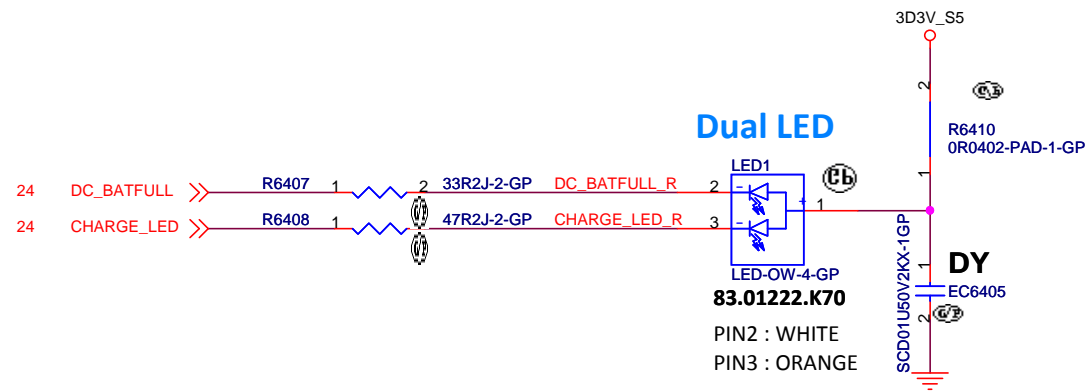


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LKL-2

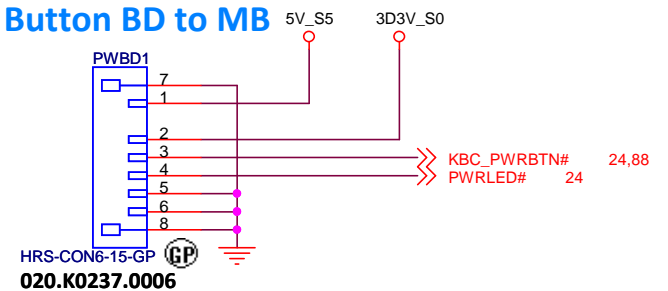
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title INT IO (RSVD)		
Size A4	Document Number Kylo-2	Rev 1M
Date: Wednesday, October 17, 2018		Sheet 62 of 99

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DC\_BATFULL\_R >> DC\_BATFULL\_R 88  
CHARGE\_LED\_R >> CHARGE\_LED\_R 88

### Power Button BD to MB



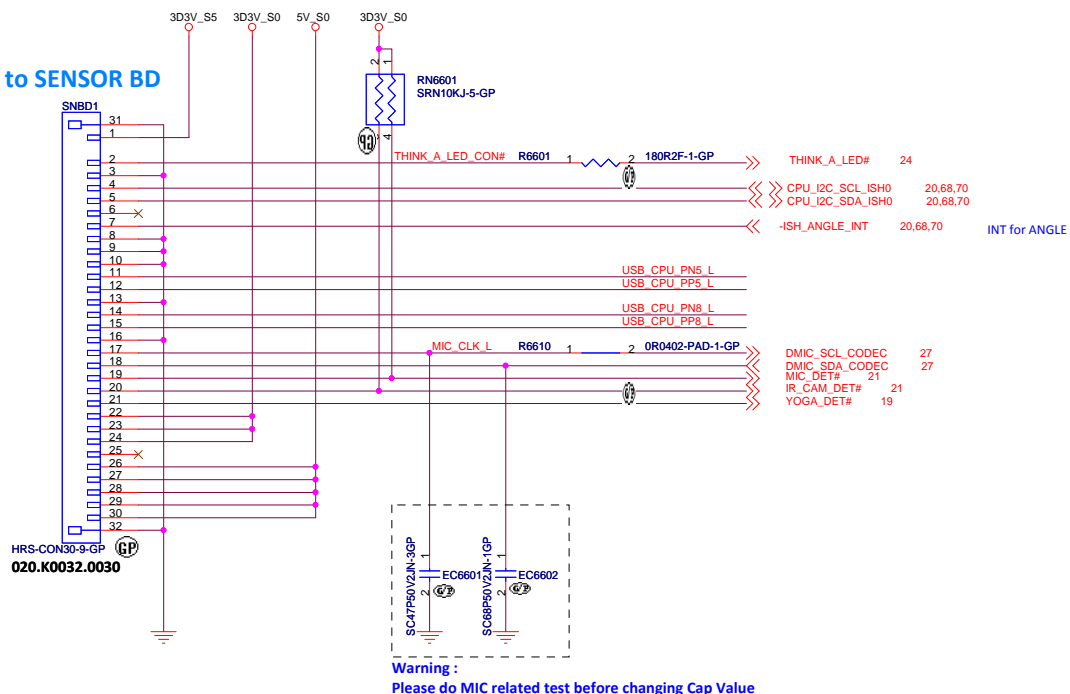
LKL-2

<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> <b>LED / BUTTON / POWER BUTTON</b>			
<b>Size</b> A4	<b>Document Number</b> <b>Kylo-2</b>		<b>Rev</b> <b>1M</b>
<b>Date:</b> Wednesday, October 17, 2018		<b>Sheet</b> 64	<b>of</b> 99

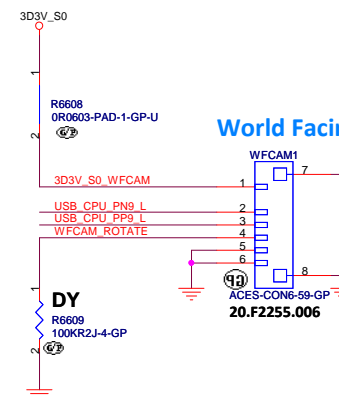




## MB to SENSOR BD



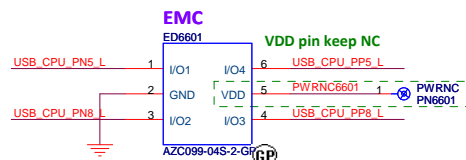
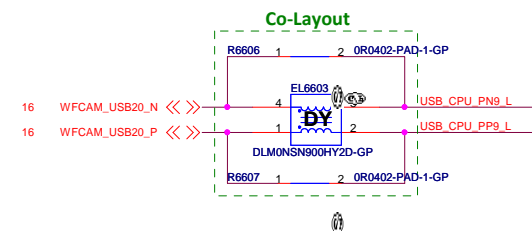
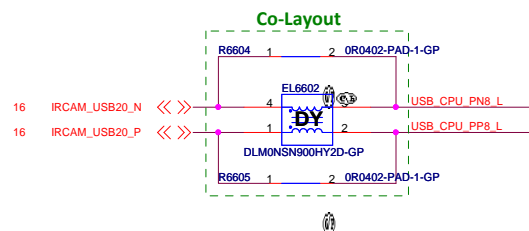
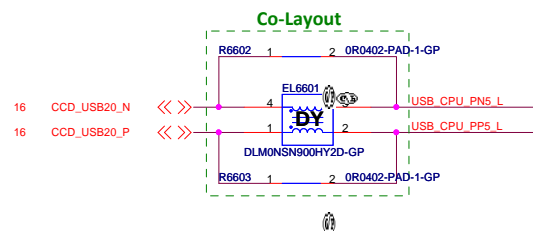
## World Facing Camera



Default camera direction is, LED on the right side of Lens/CMOS.

Pin4 supply = High : Normal image (default, and if this pin not be connected = normal image)

Pin4 supply = Low : Upside down image (means if we can rotate camera module 180 degree = LED on left side, use this mode)



LKL-2

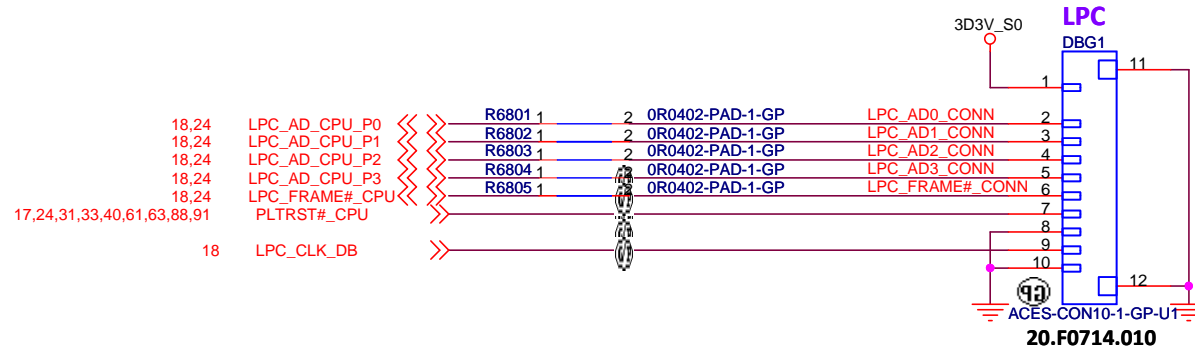
<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> <b>IO BOARD CONN (SNBD/WFCAM)</b>			
<b>Size</b> A3	<b>Document Number</b> <b>Kylo-2</b>	<b>Rev</b> <b>1M</b>	
<b>Date:</b> Wednesday, October 17, 2018		<b>Sheet</b> 66	<b>of</b> 99



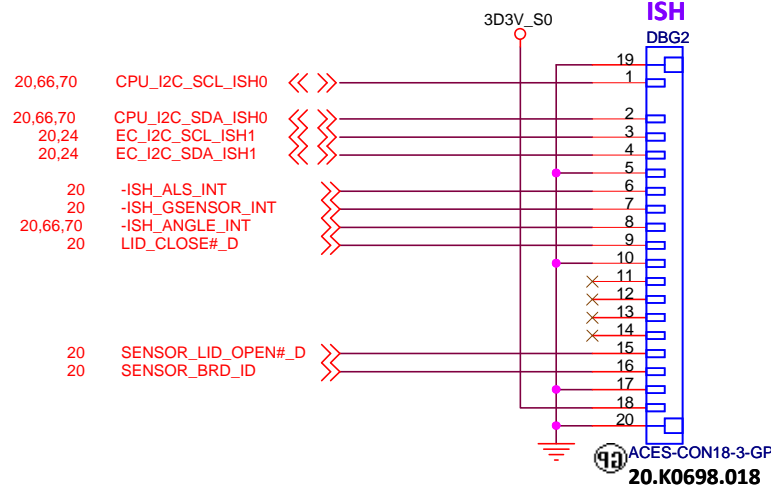
B

1

## LPC Connector



## Sensors Debug Hooks



LKL-2

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**DEBUG (LPC DEBUG)**Size  
A4

Document Number

**Kylo-2**Rev  
**1M**

Date: Wednesday, October 17, 2018

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LKL-2

<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title SENSOR (RSVD)		
Size A4	Document Number Kylo-2	Rev 1M
Date: Wednesday, October 17, 2018		Sheet 69 of 99



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LKL-2

<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <b>EXT IO (RSVD)</b>		
Size A4	Document Number <b>Kylo-2</b>	Rev <b>1M</b>
Date: Wednesday, October 17, 2018	Sheet 71 of	99

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LKL-2

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title EXT IO (RSVD)		
Size A4	Document Number Kylo-2	Rev 1M
Date: Wednesday, October 17, 2018		Sheet 72 of 99



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LKL-2

<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <b>EXT IO (RSVD)</b>		
Size A4	Document Number <b>Kylo-2</b>	Rev <b>1M</b>
Date: Wednesday, October 17, 2018	Sheet 73 of	99

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LKL-2

<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <b>EXT IO (RSVD)</b>		
Size A4	Document Number <b>Kylo-2</b>	Rev <b>1M</b>
Date: Wednesday, October 17, 2018	Sheet 74 of	99

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LKL-2

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title EXT IO (RSVD)		
Size A4	Document Number Kylo-2	Rev 1M
Date: Wednesday, October 17, 2018	Sheet 75 of	99

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LKL-2

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title GPU (RSVD)		
Size A4	Document Number Kylo-2	Rev 1M
Date: Wednesday, October 17, 2018		Sheet 76 of 99

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LKL-2

<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <b>GPU (RSVD)</b>		
Size A4	Document Number <b>Kylo-2</b>	Rev <b>1M</b>
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Title <b>GPU (RSVD)</b>		
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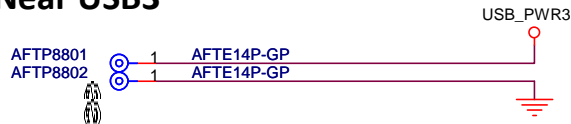
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Title <div>GPU (RSVD)</div>		
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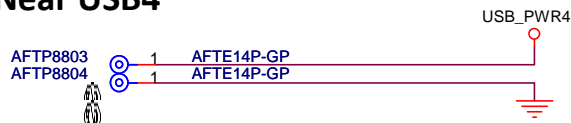
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Title <div>GPU (RSVD)</div>		
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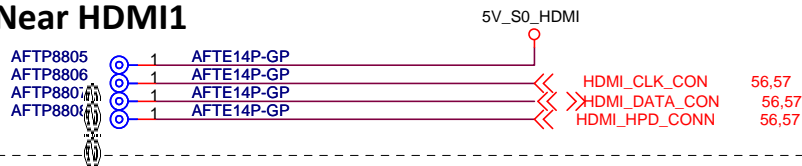
## Near USB3



## Near USB4



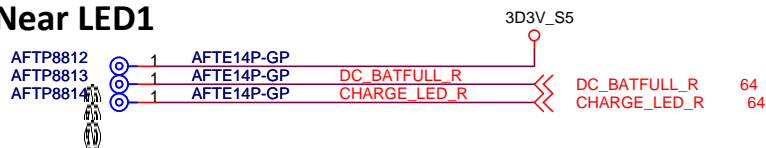
## Near HDMI1



## Near FAN1



## Near LED1

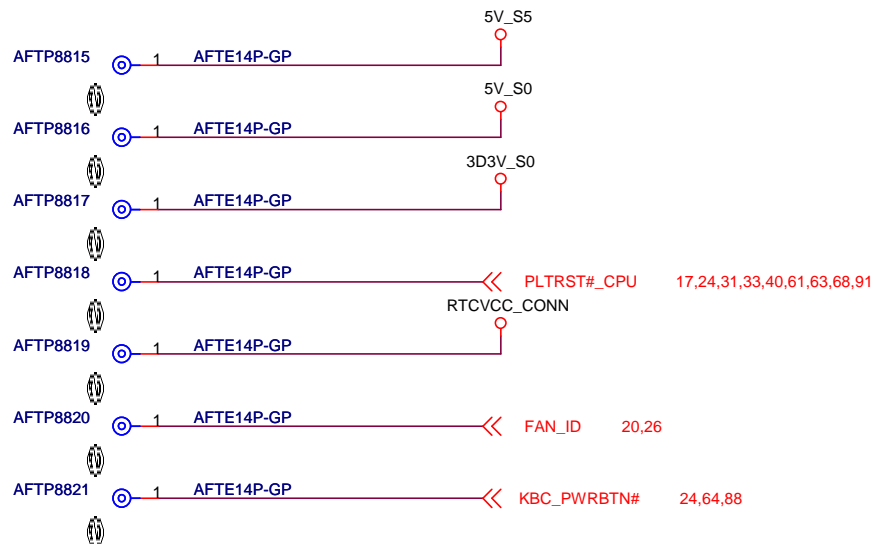


Place on top side

TP8801 1 TPAD60 << KBC\_PWRBTN# 24,64,88

TP8802 1 TPAD60 << KBC\_PWRBTN# 24,64,88

Place on bottom side



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**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**UNUSED PARTS (TEST POINT)**

Size  
A4

Document Number

**Kylo-2**

Rev  
**1M**

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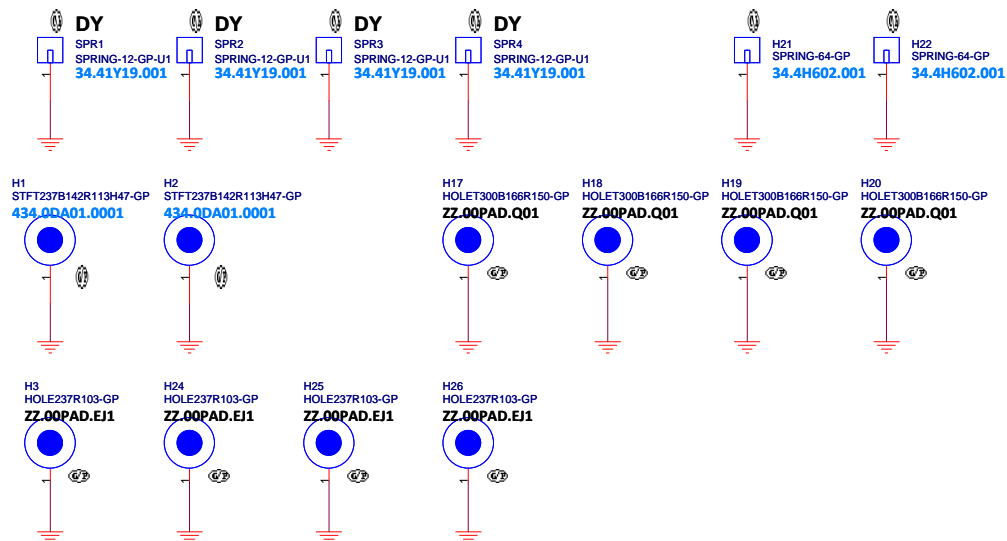
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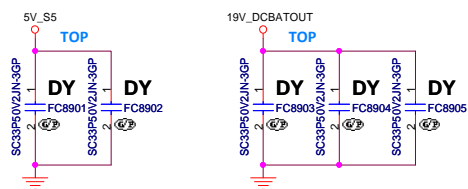


## EMI Clip

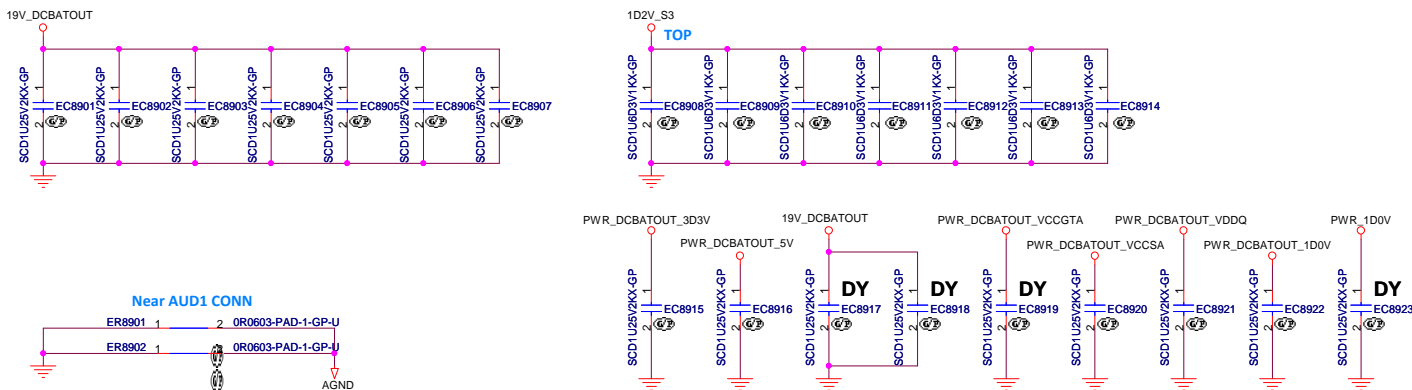
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KL2\_SVT\_MB\_W007  
KL2\_SVT\_MB\_W019



## RF Capacitors

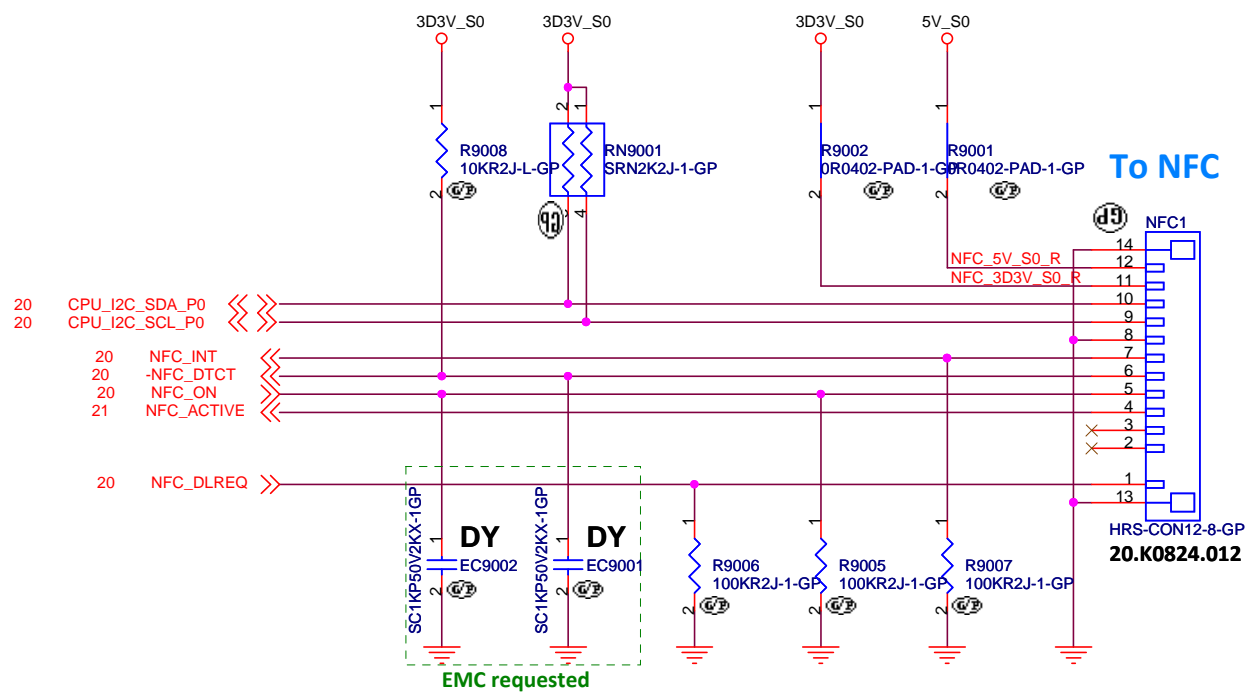


## EMI Capacitors



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<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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Pin	Symbol	Pin Type	Refer	Description
1	VBAT	Input Power	N/A	Power supply from system (4.5V - 5.5V)
2	PVDD	Input Power	N/A	Power supply to I/O (3.0V - 3.6V)
3	I2C_SDA	I/O	PVDD	I2C data
4	I2C_SCL	I	PVDD	I2C clock
5	GND	G	N/A	Ground
6	IRQ	O	PVDD	Interrupt from NFC module to the host (Host Wake)
7	NFC_Presence	G	N/A	Connect to ground for NFC module presence bit (Low active)
8	VEN	I	VBAT	Reset pin. Set the device in Hard Power Down
9	TX_PWR_REQ	O	VDD	(External TX power supply request) (Active high 1.8V level output) Indicates NFC busy state during NFC communication to touchpad.
10	PMUVCC	Input Power	N/A	Power supply to UICC(1.78V~3.3V)
11	SWIO_UICC	I/O	VDD(SIM)	SWP data connection to SIM
12	DWL_REQ	I	PVDD	Firmware download control pin
S1	GND	G	N/A	Ground
S2	GND	G	N/A	Ground

Remark: P = power supply, G = ground, I = input, O = output, I/O = input/output

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Title

INT IO (NFC)

Size A4

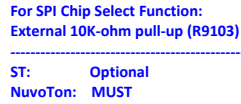
Document Number

Kylo-2

Rev 1M

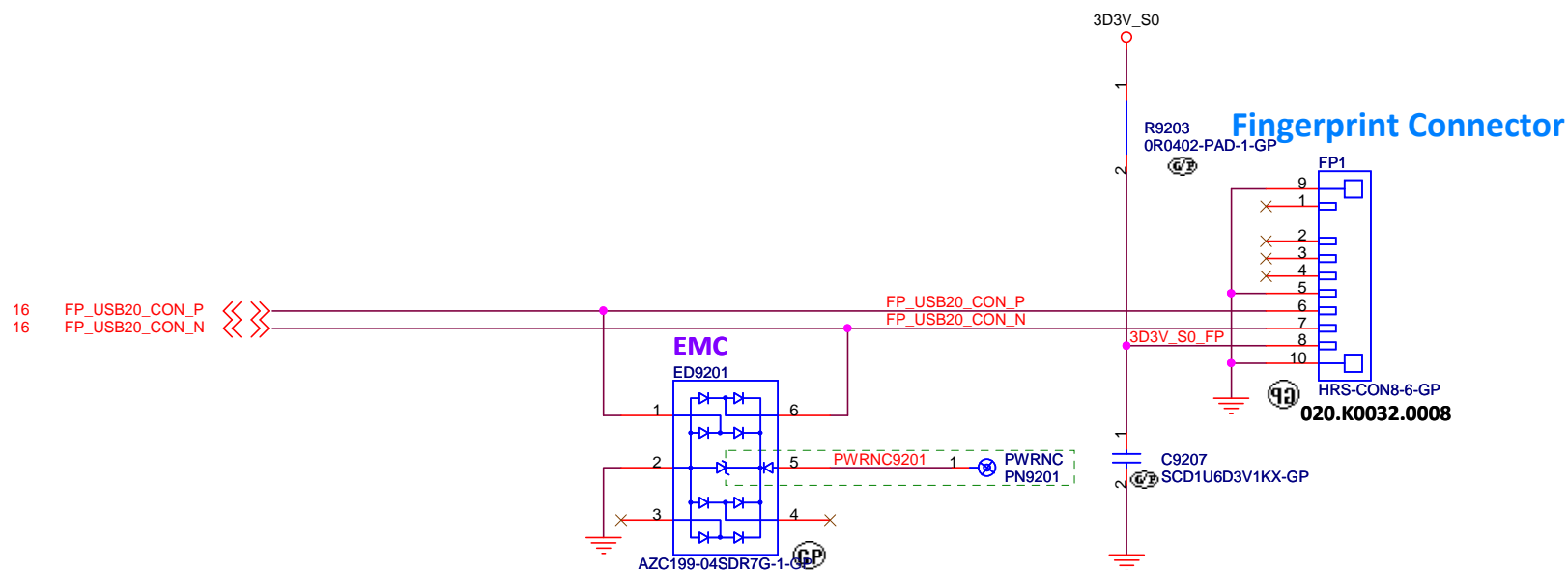
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SPI Chip Select Pin:		
ST	(SPI_CS#)	Internal pull-up
NuvoTon	(SCS#)	Internal pull-up is disabled if the pin is part of the recognized host interface

Pin No	TCG PTP Spec	ST ST33HTPH2E32AHC0	NuovoTon NPCT750LABYX	MPHear SLPB670V (22-1)-FM07-15
1	VDD	NC	VSB	VDD
2	GND	GND	NC	GND
3	GPIO	NC	NC	NC
4	GPIO	NC	PP/GPIO6	NC
5	NC	NC	NC	NC
6	NC/GPIO	GPIO	GPIO3	GPIO
7	GPIO/VDD	PP	NC	PP
8	VDD	NC	VHIO	VDD
9	GND	NC	NC	GND
10	NC/GPIO	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	NC
13	NC/GPIO	NC	GPIO4	NC
14	VDD	NC	NC	NC
15	NC	NC	NC	NC
16	GND	NC	GND	NC
17	SPI_RST#	SPI_RST#	PLTRST#	RST#
18	SPI_PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2	PIRQ#
19	SPI_CLK	SPI_CLK	SCLK	SCLK
20	SPI_CS#	SPI_CS#	SCS#/GPIO5	CS#
21	MOSI	MOSI	MOSI/GPIO7	MOSI
22	VDD	VPS	VHIO	VDD
23	GND	NC	GND	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	NC
28	NC	NC	NC	NC
29	NC/GPIO	NC	SDA/GPIO0	NC
30	NC/GPIO	NC	SCL/GPIO1	NC
31	NC	NC	NC	NC
32	GND	NC	NC	GND



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<p>Title <b>INT IO (FINGERPRINT)</b></p>	
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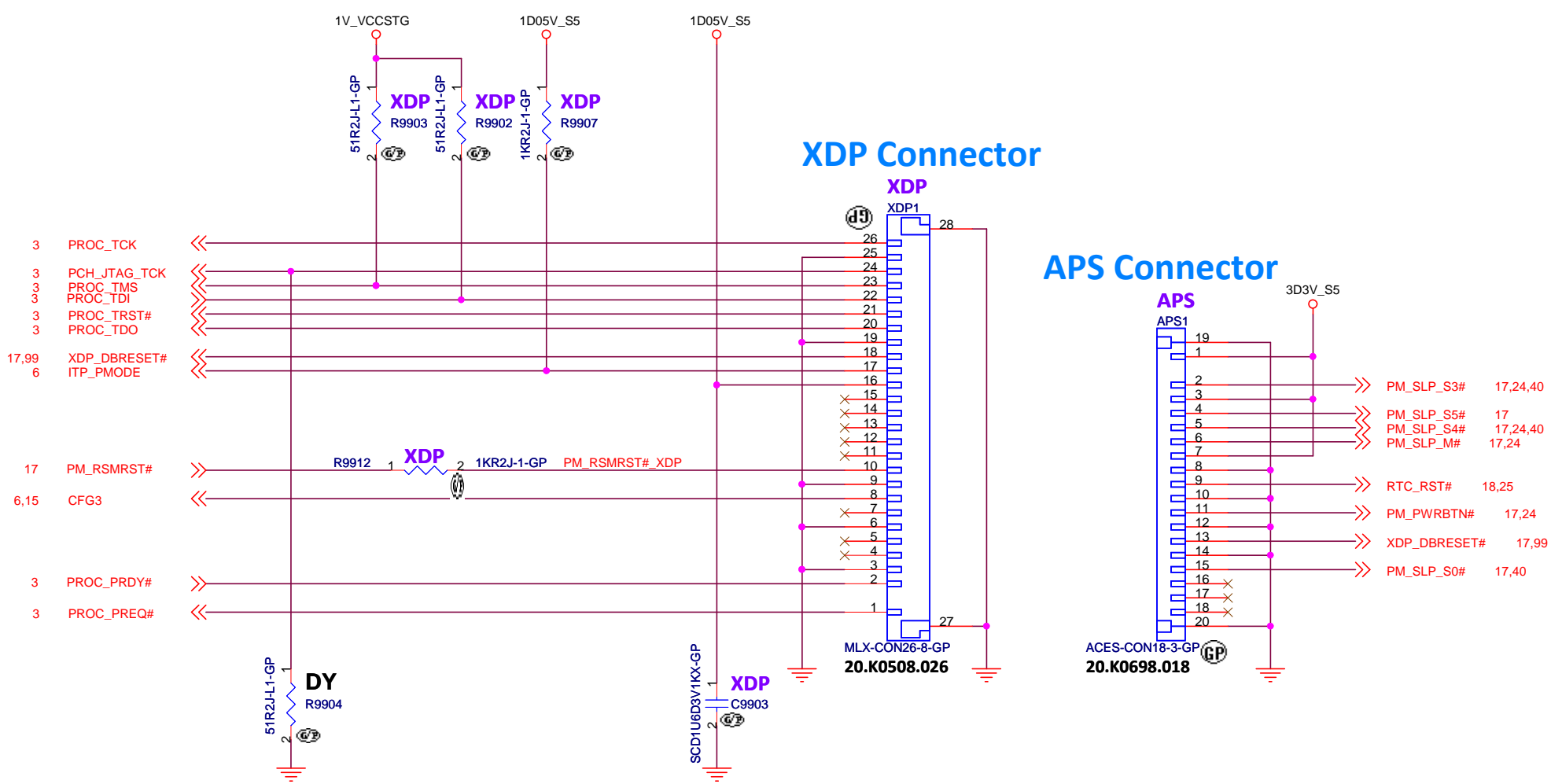
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Title <b>DEBUG (XDP/APS)</b>			
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